H1 Very Forward Proton Spectrometer

Coincidence Unit

Preliminary !

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Content

Introduction

The VFPS Coincidence Unit has been developed in order to have a hit rate monitor for the Roman Pots of the Very Forward Proton Spectrometer. Hit rate observation is of particular importance, when moving the detectors close to beam.
The Coincidence Unit accepts as inputs the digital comparator signals of the Pot's trigger tiles, combines them in different logical equations, which are defined by firmware, and provides the logical results as digital ECL signals at two output connectors.
Additionally an oscillator with programmable divider has been implemented, which can be used as time base for the rate measurement.
The Module has been designed as VME Board of 6 height units, which uses connector P1 only for power supply.

Block Diagram

Fig.1 shows a block diagram of the Coincidence Unit. On the left side 16 digital comparator signals of the trigger tiles of POT220 and POT224 each are connected to flat cable connectors P3 and P4 respectively.

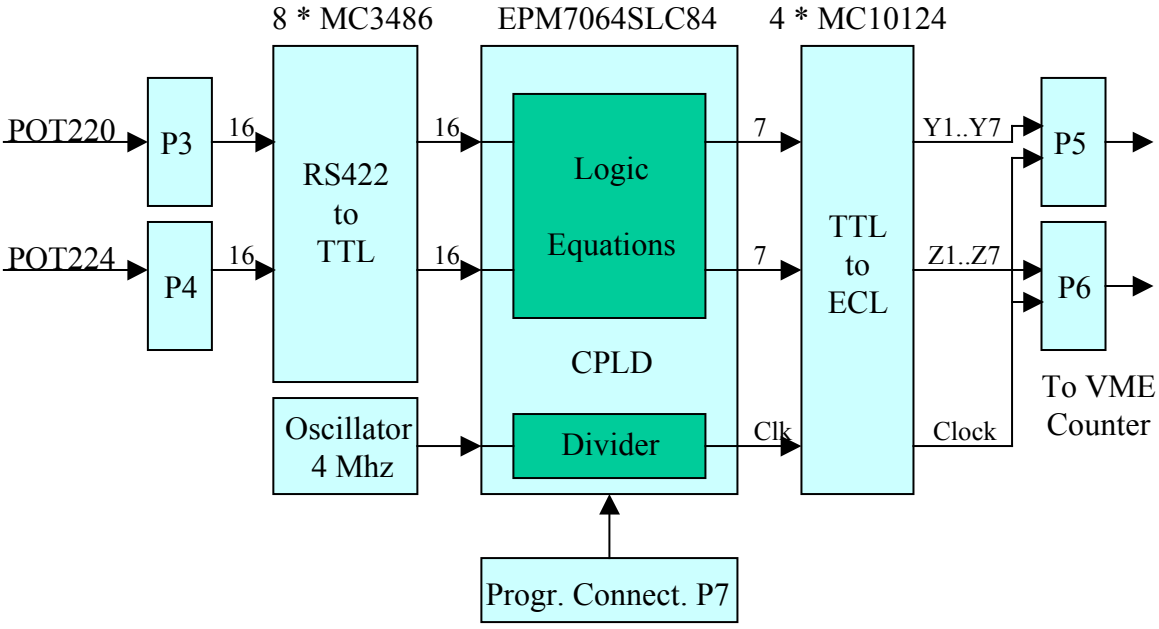
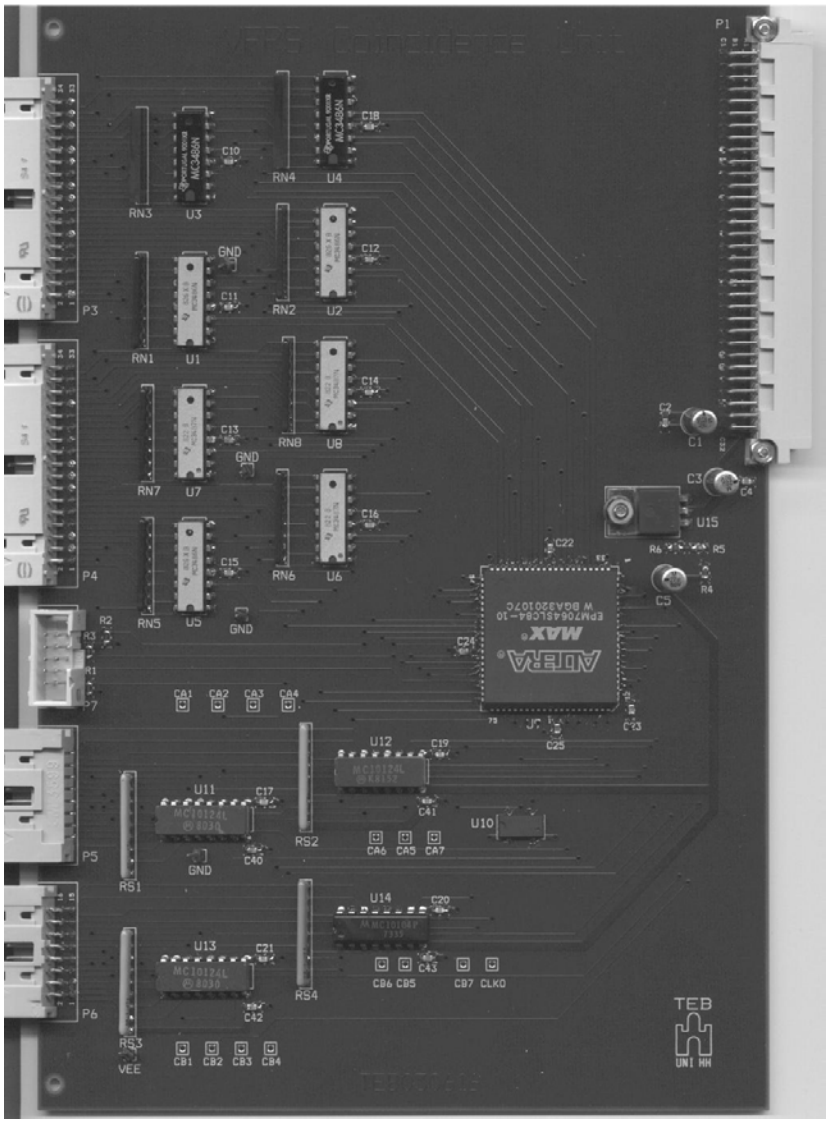


Fig. 1: VFPS Coincidence Unit Block Diagram

After conversion from RS422 to TTL they are routed to a CPLD of type EPM7064SLC84 (Altera). Here two groups of seven free programmable logical combinations of the 32 inputs signals are implemented. The programming of the firmware can be done in situ by a laptop connected to P7.
Additionally a programmable divider is provided, which generates from a 4 MHz oscillator a frequency **CLK** as time base for rate measurements. The actual programming of the CPLD is documented in the appendix.
Two groups of seven logic result signals (Y1..Y7 and Z1..Z7) and the **CLK** signal are converted to ECL and distributed to two output connectors P5 and P6, which match – concerning pin numbering and signal level – to the input connectors of the C.A.E.N counter module Model V560E.
So operating the VFPS coincidence Unit together with Model V560E provides a multiple rate meter for flexible logical combinations of detector signals.

Appendix

1) Board Layout



2) Front Panel

Connector	Type	Function
P3	34 pin lead flat cable	Input A (POT220)
P4	34 pin lead flat cable	Input B (POT224)
P5	16 pin lead flat cable	Output Y1..Y7, Clock
P6	16 pin lead flat cable	Output Z1..Z7, Clock
P7	10 pin lead flat cable	CPLD Programming

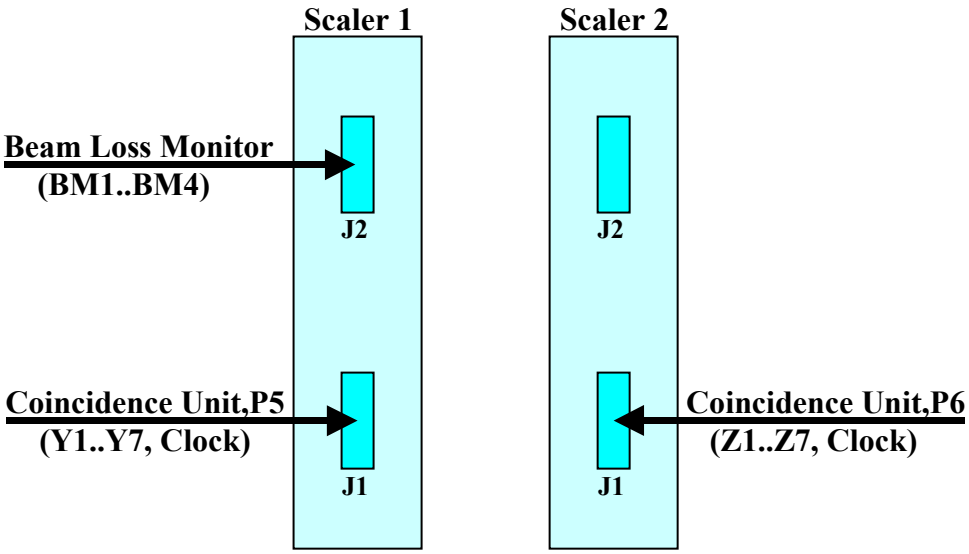
3) Input Connectors P3, P4

Pin Number	Signal Name	Tile Detector
1	T1a~	Layer 1, Tile a
2	T1a	
3	T1b~	Layer 1, Tile b
4	T1b	
5	T1c~	Layer 1, Tile c
6	T1c	
7	T1d~	Layer 1, Tile d
8	T1d	
9	T2a~	Layer 2, Tile a
10	T2a	
11	T2b~	Layer 2, Tile b
12	T2b	
13	T2c~	Layer 2, Tile c
14	T2c	
15	T2d~	Layer 2, Tile d
16	T2d	
17	T3a~	Layer 3, Tile a
18	T3a	
19	T3b~	Layer 3, Tile b
20	T3b	
21	T3c~	Layer 3, Tile c
22	T3c	
23	T3d~	Layer 3, Tile d
24	T3d	
25	T4a~	Layer 4, Tile a
26	T4a	
27	T4b~	Layer 4, Tile b
28	T4b	
29	T4c~	Layer 4, Tile c
30	T4c	
31	T4d~	Layer 4, Tile d
32	T4d	

4) Output Connectors P5, P6

Coincidence Unit			C.A.E.N V560E, Nr.1		Coincidence Unit		C.A.E.N V560E, Nr.2	
Pin Nr.	Connector	Signal	Connector	Counter	Connector	Signal	Connector	Counter
1	P5	Y1	J1	1	P6	Z1	J1	1
2	P5	Y1~	J1		P6	Z1~	J1	
3	P5	Y2	J1	2	P6	Z2	J1	2
4	P5	Y2~	J1		P6	Z2~	J1	
5	P5	Y3	J1	3	P6	Z3	J1	3
6	P5	Y3~	J1		P6	Z3~	J1	
7	P5	Y4	J1	4	P6	Z4	J1	4
8	P5	Y4~	J1		P6	Z4~	J1	
9	P5	Y5	J1	5	P6	Z5	J1	5
10	P5	Y5~	J1		P6	Z5~	J1	
11	P5	Y6	J1	6	P6	Z2	J1	6
12	P5	Y6~	J1		P6	Z6~	J1	
13	P5	Y7	J1	7	P6	Z7	J1	7
14	P5	Y7~	J1		P6	Z7~	J1	
15	P5	CLK	J1	8	P6	CLK	J1	8
16	P5	CLK~	J1		P6	CLK~	J1	

5) Rate Monitor System



6) CPLD Program

```
SUBDESIGN coincidence
        (
        CLKIN                                   :INPUT;         % Input Clock %
        TA1A~,TA1B~,TA1C~,TA1D~                 :INPUT;         % 1.Plane of first Pot %
        TA2A~,TA2B~,TA2C~,TA2D~                 :INPUT;         % 2.Plane of first Pot %
        TA3A~,TA3B~,TA3C~,TA3D~                 :INPUT;         % 3.Plane of first Pot %
        TA4A~,TA4B~,TA4C~,TA4D~                 :INPUT;         % 4.Plane of first Pot %
        TB1A~,TB1B~,TB1C~,TB1D~                 :INPUT;         % 1.Plane of second Pot %
        TB2A~,TB2B~,TB2C~,TB2D~                 :INPUT;         % 2.Plane of second Pot %
        TB3A~,TB3B~,TB3C~,TB3D~                 :INPUT;         % 3.Plane of second Pot %
        TB4A~,TB4B~,TB4C~,TB4D~                 :INPUT;         % 4.Plane of second Pot %

        Y[7..1]                                 :OUTPUT;        % Logical Results, 1. Connector %
        Z[7..1]                                 :OUTPUT;        % Logical Results, 2. Connector %
        CLKOUT                                  :OUTPUT;        % Output Clock %
        )
VARIABLE
        LA1,LA2,LA3,LA4                         :LCELL;         % Layers of first Pot %
        LB1,LB2,LB3,LB4                         :LCELL;         % Layers of second Pot %
        CD[1..0]                                :TFF;           % Clock Divider %

Begin
%**************************** Clock Generation *****************************%
        CD[0].T = VCC;
        CD[1].T = CD[0];
        CD[1..0].clk = CLKIN;                   % CLKIN: 4 MHz %
        CLKOUT = CD[1];                         % CLKOUT: 1 MHz %
%**************************** Layer Definition *****************************%
        LA1 = !TA1A~ # !TA1B~ # !TA1C~ # !TA1D~;
        LA2 = !TA2A~ # !TA2B~ # !TA2C~ # !TA2D~;
        LA3 = !TA3A~ # !TA3B~ # !TA3C~ # !TA3D~;
        LA4 = !TA4A~ # !TA4B~ # !TA4C~ # !TA4D~;
        LB1 = !TB1A~ # !TB1B~ # !TB1C~ # !TB1D~;
        LB2 = !TB2A~ # !TB2B~ # !TB2C~ # !TB2D~;
        LB3 = !TB3A~ # !TB3B~ # !TB3C~ # !TB3D~;
        LB4 = !TB4A~ # !TB4B~ # !TB4C~ # !TB4D~;
%**************************** Output Definition ****************************%
        Y[1] = LA1 & LA2 & LA3 & LA4;                           % 4 out 4, first Pot %
        Y[2] = LA1 & LA2 & LA3 # LA1 & LA2 & LA4                % 3 out 4, first Pot %
             # LA1 & LA3 & LA4 # LA2 & LA3 & LA4;
        Y[3] = LA1 & LA2 # LA1 & LA3 # LA1 & LA4                % 2 out 4, first Pot %
             # LA2 & LA3 # LA2 & LA4 # LA3 & LA4;
        Y[4] = LB1 & LB2 & LB3 & LB4;                           % 4 out 4, second Pot %
        Y[5] = LB1 & LB2 & LB3 # LB1 & LB2 & LB4                % 3 out 4, second Pot %
             # LB1 & LB3 & LB4 # LB2 & LB3 & LB4;
        Y[6] = LB1 & LB2 # LB1 & LB3 # LB1 & LB4                % 2 out 4, second Pot %
             # LB2 & LB3 # LB2 & LB4 # LB3 & LB4;
        Y[7] = Y[3] & Y[6];

        Z[1] = LA1;
        Z[2] = LA2;
        Z[3] = LA3;
        Z[4] = LA4;
        Z[5] = LB1;
        Z[6] = LB2;
        Z[7] = LB3 # LB4;
End;
```