High Pt Pretrigger Electronics

Link Board

H. Riege, J. Schütt, R. van Staa
Universität Hamburg

II. Institut für Experimentalphysik
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Attention !

The Link Board is equipped with Laser Diodes class 3b.

The laser light is not visible (wavelength: 825 nm)

It should be treated as potential hazard.

Do not look into the Laser Diode !!

Content

Introduction

The High-Pt Pretrigger Electronics is built of three different boards:

- The Link Board **LB**, which is located near the detector and provides via optical fibres the fast data transfer to the main trigger logic.
- The Pretrigger Board **PB**, which searches for coincidence pattern as trigger candidates and combines the involved pad information of three detector layers to data sets, which are transmitted to the third board,
- The Message Generator **MG**, which transforms the received data to messages, which are accepted by the Track Finding Unit **TFU** of the HERA-B First Level Trigger System.

This Manual describes the Link Board, which has two main goals:

- Acceptance of all 256 pixel information of a Front End Driver Board FED
- Transmission of all pixels of a pair of half detector rows on one link channel.

Since the length of half a detector row varies between 32 and 48 pixels, these two requirements cannot met by only one type of Link Board. So two different layouts have been designed, the first one (Type A) with four link channels for a constant row length of 32 bits each, and a second one with three link channels of row length between 36 and 48 bits each. This one can be configured by means of three jumpers to different types (B, B*, C, D).

The Link Board has been designed as a piggyback card, which is screwed directly onto a FED board (see Assembly of FED and Link Board in the appendix). For that purpose the FED output connectors have to be replaced by female ones.

Logic Description

One link channel on the Link Board has to transmit the data of two half detector rows during one bunch crossing interval of 96 nsec. Therefore at first the incoming data have to be stored in registers.

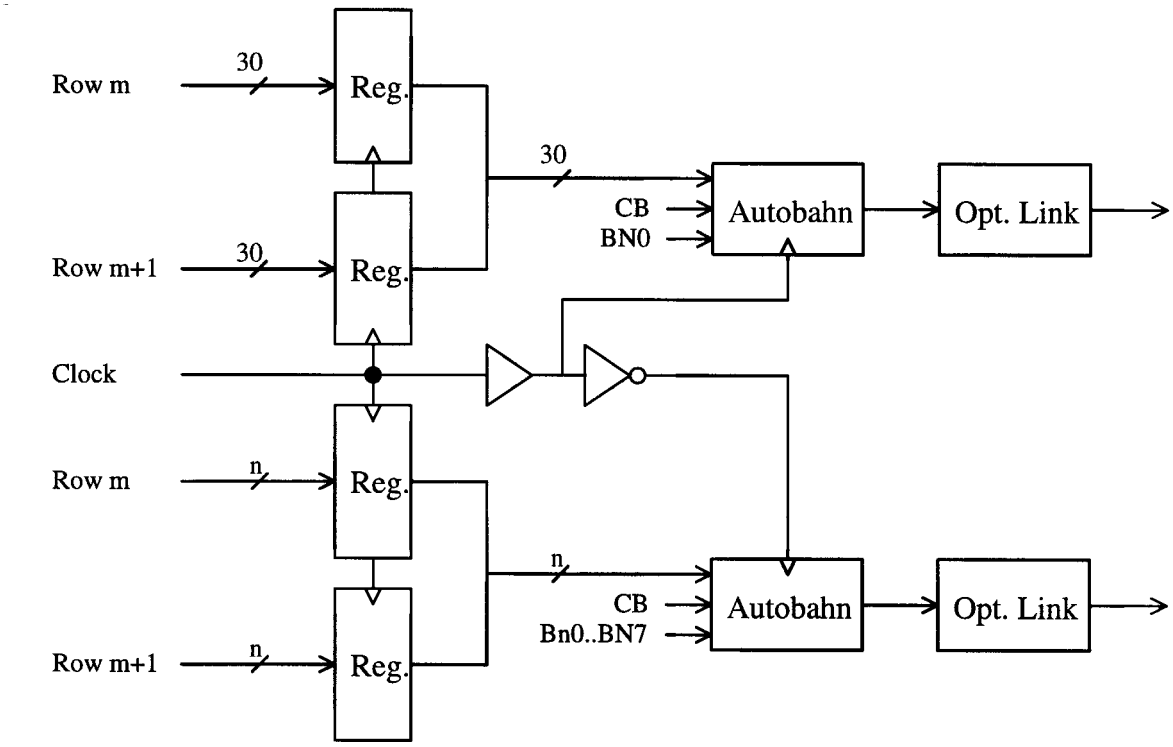


Fig.1: Block Diagram of one Link Board Channel

The register outputs are multiplexed to Autobahn transmitters with a period of 48 nsec. Each link consists of two transmitters, the first one sending the first 30 pixel bits, a Cycle Bit **CB** and the least significant Bunch Number bit **BN0**, while the second one transmits the remaining pixel bits, the Cycle Bit and the complete 8 bit Bunch Number. Unused bits are forced to 0. The Cycle Bit distinguishes between the first and the second data set transmitted. The board is operating completely synchronously with the Bunch Clock.

The different board types are shortly described in the following. A logic diagram of one link channel of each type can be found in the appendix. The pixel in general are numbered from the centre to the border of the detector.

Type A

Link Board type A is used in sections A of the inner and outer detector part. (For detector sections see the corresponding figures in the appendix.) It provides four link channels for pairs of half rows with 32 pixels each. The correspondence between detector rows, FED input connectors and link channels is shown in the following table:

Row Num.	Pixel Num.	Input Connector	Link Channel
m	0..15	1 a	1
m	16..31	1 b	1
m+1	0..15	2 a	1
m+1	16..31	2 b	1
m+2	0..15	3 a	2
m+2	16..31	3 b	2
m+3	0..15	4 a	2
m+3	16..31	4 b	2
m+4	0..15	5 a	3
m+4	16..31	5 b	3
m+5	0..15	6 a	3
m+5	16..31	6 b	3
m+6	0..15	7 a	4
m+6	16..31	7 b	4
m+7	0..15	8 a	4
m+7	16..31	8 b	4

Table 1: Correspondence between Detector Rows, FED Inputs and Link Channels on Link Board Type A

Type B

Link Board type B is used in sections B of the inner detector part. (For detector sections see the corresponding figures in the appendix.) It provides three link channels for pairs of half rows with 40 pixels each. The correspondence between detector rows, FED input connectors and link channels is shown in the following table:

Row Num.	Pixel Num.	Input Connector	Link Channel
m	0..15	1 a	1
m	16..31	1 b	1
m	32..39	7 a (P1..P8)	1
m+1	0..15	2 a	1
m+1	16..31	2 b	1
m+1	32..39	7 a (P9..P16)	1
m+2	0..15	3 a	2
m+2	16..31	3 b	2
m+2	32..39	7 b (P1..P8)	2
m+3	0..15	4 a	2
m+3	16..31	4 b	2
m+3	32..39	7 b (P9..P16)	2
m+4	0..15	5 a	3
m+4	16..31	5 b	3
m+4	32..39	8 a (P1..P8)	3
m+5	0..15	6 a	3
m+5	16..31	6 b	3
m+5	32..39	8 a (P9..P16)	3

Table 2: Correspondence between Detector Rows, FED Inputs and Link Channels on Link Board Type B

The pixel data received on input connector 8b are not processed on this board, but transmitted to a Link Board of type C via a dedicated Link Interconnect **LIC** (see board layout in the appendix).

Type B*

Link Board type B* is used only for section B* of the outer detector part. (For detector sections see the corresponding figures in the appendix.) It provides one link channels for pairs of half rows with 48 pixels each and two link channels for pairs of half rows with 32 pixels each. The correspondence between detector rows, FED input connectors and link channels is shown in the following table:

Row Num.	Pixel Num.	Input Connector	Link Channel
m	0..15	1 a	1
m	16..31	1 b	1
m	32..47	7 a	1
m+1	0..15	2 a	1
m+1	16..31	2 b	1
m+1	32..47	7 b	1
m+2	0..15	3 a	2
m+2	16..31	3 b	2
m+3	0..15	4 a	2
m+3	16..31	4 b	2
m+4	0..15	5 a	3
m+4	16..31	5 b	3
m+5	0..15	6 a	3
m+5	16..31	6 b	3

Table 3: Correspondence between Detector Rows, FED Inputs and Link Channels on Link Board Type B*

The pixel data received on input connectors 8a and 8b are not processed on this board, but transmitted to a Link Board of type C via a dedicated Link Interconnect **LIC** (see board layout in the appendix).

Type C

Link Board type C is used in sections C of the inner and outer detector part. (For detector sections see the corresponding figures in the appendix.) It provides three link channels for pairs of half rows with 48 pixels each. The correspondence between detector rows, FED input connectors and link channels is shown in the following table:

Row Num.	Pixel Num.	Input Connector	Link Channel
m	0..15	1 a	1
m	16..31	1 b	1
m	32..47	7 a	1
m+1	0..15	2 a	1
m+1	16..31	2 b	1
m+1	32..47	7 b	1
m+2	0..15	3 a	2
m+2	16..31	3 b	2
m+2	32..47	8 a	2
m+3	0..15	4 a	2
m+3	16..31	4 b	2
m+3	32..47	8 b	2
m+4	0..15	5 a	3
m+4	16..31	5 b	3
m+4	32..47	LIC [1)]	3
m+5	0..15	6 a	3
m+5	16..31	6 b	3
m+5	32..47	LIC [2)]	3

Table 4: Correspondence between Detector Rows, FED Inputs and Link Channels on Link Board Type C

The pixels Num. 32..47 of the last two rows are not provided by the input connectors, but by the dedicated Link Interconnect **LIC** (see board layout in the appendix).

LIC [1)] : Signals are coming from Connector 8b of Link Board B or from Connector 8a of Link Board B[*].
LIC [2)] : Signals are coming from Connector 8b of Link Board D or from Connector 8b of Link Board B[*].

Type D

Link Board type D is used in sections D of the inner detector part. (For detector sections see the corresponding figures in the appendix.) It provides three link channels for pairs of half rows with 36 pixels each. The correspondence between detector rows, FED input connectors and link channels is shown in the following table:

Row Num.	Pixel Num.	Input Connector	Link Channel
m	0..15	1 a	1
m	16..31	1 b	1
m	32..35	7 a (P1..P4)	1
m+1	0..15	2 a	1
m+1	16..31	2 b	1
m+1	32..35	7 a (P9..P12)	1
m+2	0..15	3 a	2
m+2	16..31	3 b	2
m+2	32..35	7 b (P1..P4)	2
m+3	0..15	4 a	2
m+3	16..31	4 b	2
m+3	32..35	7 b (P9..P12)	2
m+4	0..15	5 a	3
m+4	16..31	5 b	3
m+4	32..35	8 a (P1..P4)	3
m+5	0..15	6 a	3
m+5	16..31	6 b	3
m+5	32..35	8 a (P9..P12)	3

Table 5: Correspondence between Detector Rows, FED Inputs and Link Channels on Link Board Type D

The pixel data received on input connector 8b are not processed on this board, but transmitted to a Link Board of type C via a dedicated Link Interconnect **LIC** (see board layout in the appendix).

Jumpers

The Link Boards of type B, B*, C and D are realised with the same board layout. They are distinguished by means of three jumpers. Link Board A has a different board layout and needs no jumpers for type selection. The following table shows the different board types with Type Number and jumper configuration.

Board Type	Type Number	Jumper JP92	Jumper JP91	Jumper JP111
A	1	Not implemented	Not implemented	Not implemented
B	0	closed	closed	closed
B*	4	open	closed	closed
C	5	closed	open	closed
D	2	open	closed	open

Table 6: Jumper Configuration and Type Number for all Link Board Types.

For convenience this table is printed on the board too. The location of the jumpers is indicated in the layout figure, which can be found in the appendix.

Board Initialisation

After power-on the state machines on the Link Board are reset to ground state. The Autobahn transmitters are initialised only after switching on the system clock on the FED Board. An initialisation cycle is started also by a FCS system reset.

Data transmission can be stopped by setting the FCS control bit STROBE6. It is strongly recommended to interrupt data transmission during initialisation of the Pretrigger Boards connected.

Test Facilities

On the Link Board a Test Mode has been implemented, which is entered by setting the FCS control bit STROBE7. In Test Mode the Link Board always sends the same data, containing besides some control information two test pattern, which consist of alternating 0 and 1. The pattern sent in the first transfer cycle (Cycle Bit = 0) starts with 0 as the least significant bit, while the second pattern (Cycle Bit = 1) has a 1 as least significant bit.

The bit allocation of the data is shown in the following table:

Bit Num.	1. Autobahn	Bit Num.	2. Autobahn
0..15	Test Pattern	0..22	0
16..29	1	23	Cycle Bit
		24	Channel Num. MSB
		25..27	Board Type
30	Cycle Bit	28..30	Board Address
31	Channel Num. MSB	31	Channel Num. LSB

Table 7: Bit Allocation in Test Mode

The Link Channel Num. is a 2 bit number, which identifies the different channels on the board (see tables 1-5). The Board Type is numbered according to table 6. The Board Address is a 3 bit identification, which can be selected by means of a hexadecimal switch on the board (the most significant bit of that switch is not used).

The following steps of test are recommended:

a) System Clock

After initialisation and data transfer start (see Board Initialisation) one should check the system clock of the Pretrigger Board, which is derived from the Handshake signals of the Autobahn receivers. If the system clock fails, one can conclude, that at least one data link is not working correctly. The faulty link(s) can be detected by systematically masking one link after the other by means of the Clock Mask Register on the Pretrigger Board. This test can be done in Normal Mode and in Test Mode.

b) Bunch Number Comparison

An appropriate test of the data integrity is the Bunch Number comparison (see Status Register of the Pretrigger Board). If some comparison bits are indicating failure, one easily can detect again not working links by using the BXN Error Mask Register on the Pretrigger Board. This test can only be done in Normal Mode.

c) Bit Test

An individual test of the first 15 pixel bits can be performed by masking all input bits on the Pretrigger Board with the exception of one single bit (on all layers) of this group. After setting the Link Boards to test Mode, one should observe in the Pretrigger Board's Test FIFO only the road corresponding to the unmasked bits in the three detector layers. This is especially a test of the first transmitter of the link channels involved.

d) Connection Test

In order to verify the correct connections between Link Boards and Pretrigger Boards one could for example define for each detector section an individual identification number, which is used as Board Address for the Link Board connected. After switching the Link Boards to

Test Mode the Link Channel Number, the Board Type and the Board Address are now occupying bits 24-31 of the 2. Autobahn transmitter and therefore are stored as Bunch Number in the Pretrigger Board's test FIFO, where it can be compared with the expected values. By means of the BXN MUX Register on the Pretrigger Board one can select, the data of which channel are written to the FIFO. Since these data are transmitted by the second connection of a link channel, this check is also a special test for the second half of the link channels involved.

Pixel Allocation

Left and right side of the inner detector part are completely symmetric. A schematic view of the pixel configuration and numbering is shown in the appendix for the right side. As one can see, the detector is subdivided into 8 sections, each covered by one Link Board. A detailed allocation of 16 bit pixel groups of all detector rows to FED's and Link Boards is given by a table in the appendix. It should be noted, that Link Board C gets one pixel group from Link Board B and one from Link Board D via the Link Interconnect **LIC**.

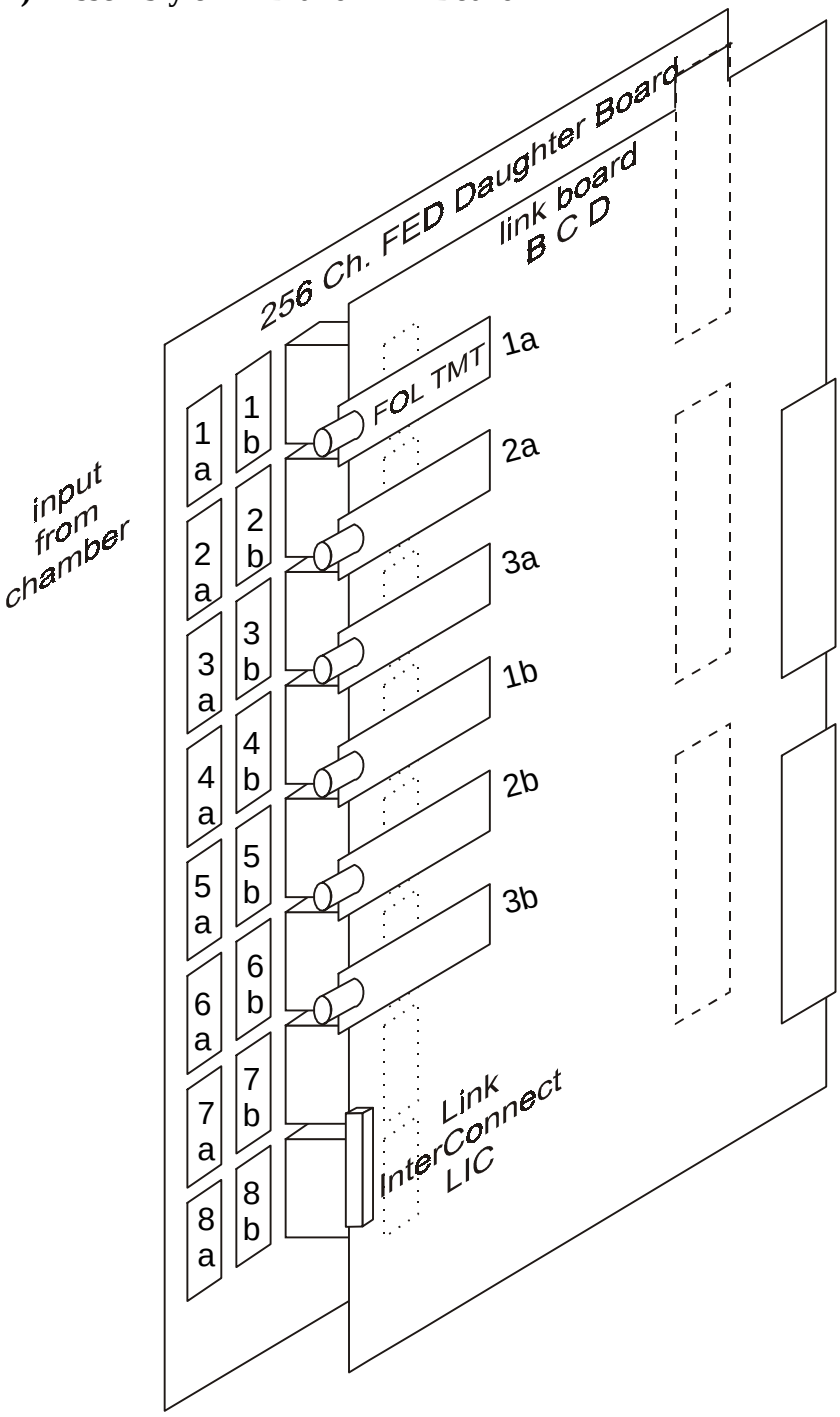
For the inner detector one needs 16 Link Boards per layer and therefore 48 Link Boards in total.

The outer part of the detector consists of 28 rows on the right side and 25 rows on the left side. The sections of both sides are shown schematically in the appendix. The corresponding Pixel Allocation Tables of both sides are given too. Here Link Board C gets two 16 bit pixel groups from Link Board B^* via Link Interconnect **LIC**.

On the right side the outer detector needs five Link Boards per layer and therefore 15 Link Boards in total. On the left side each layer needs 4 Link Boards in the sequence D_1, C_1, D_2, C_2. Additionally row #23 of the first two layers is covered by Link Board C_3 and row #23 of the third layer is connected to Link Board C_4. Therefore for the complete left side 14 Link Boards are necessary.

Appendix

1) Assembly of FED and Link Board

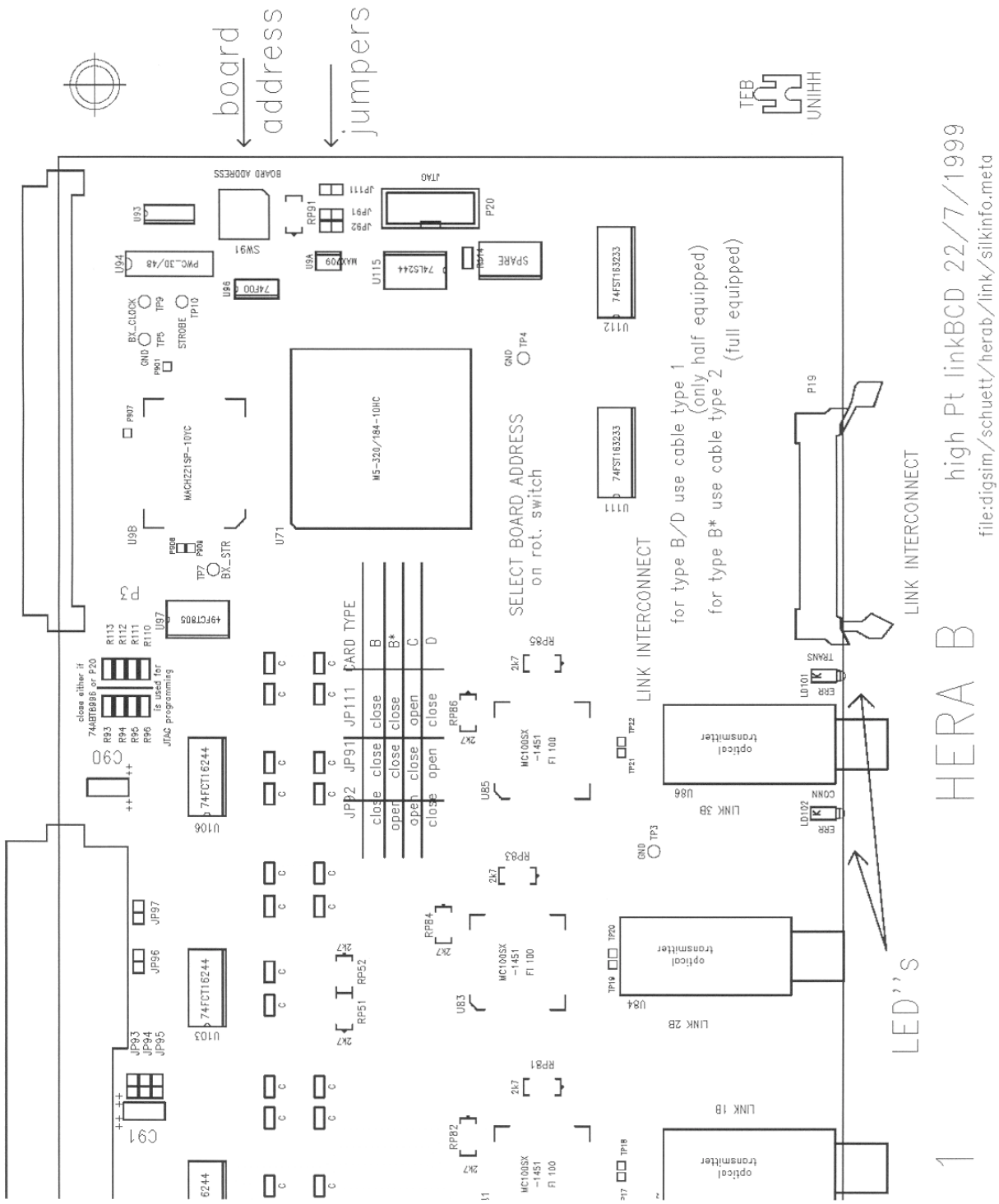


link board - FED board assembly

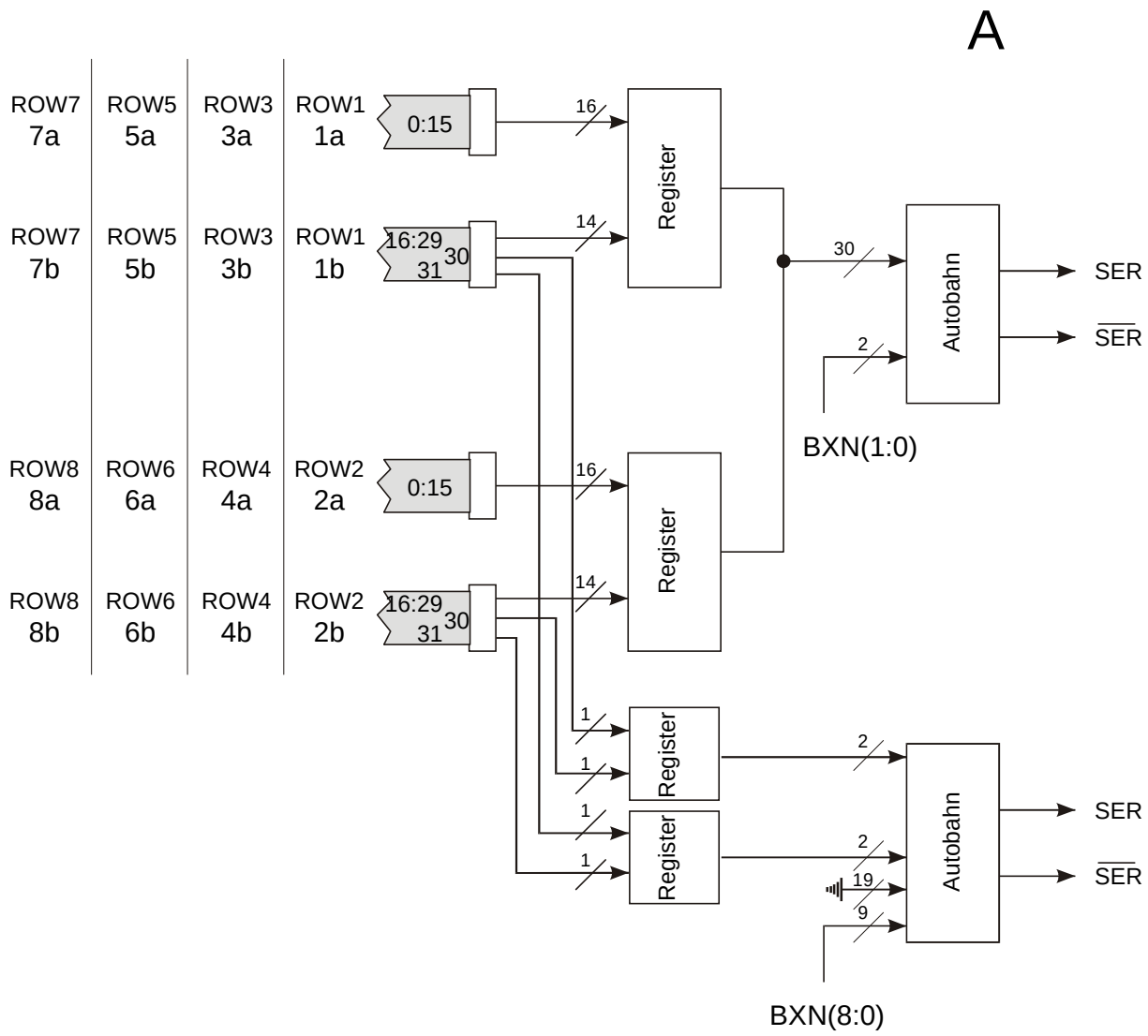
LINK-BOARD Detail

Proj. HERA-B

2) Board Layout: Jumpers and Board Address Switch



3) Logic Diagram of Link Board A

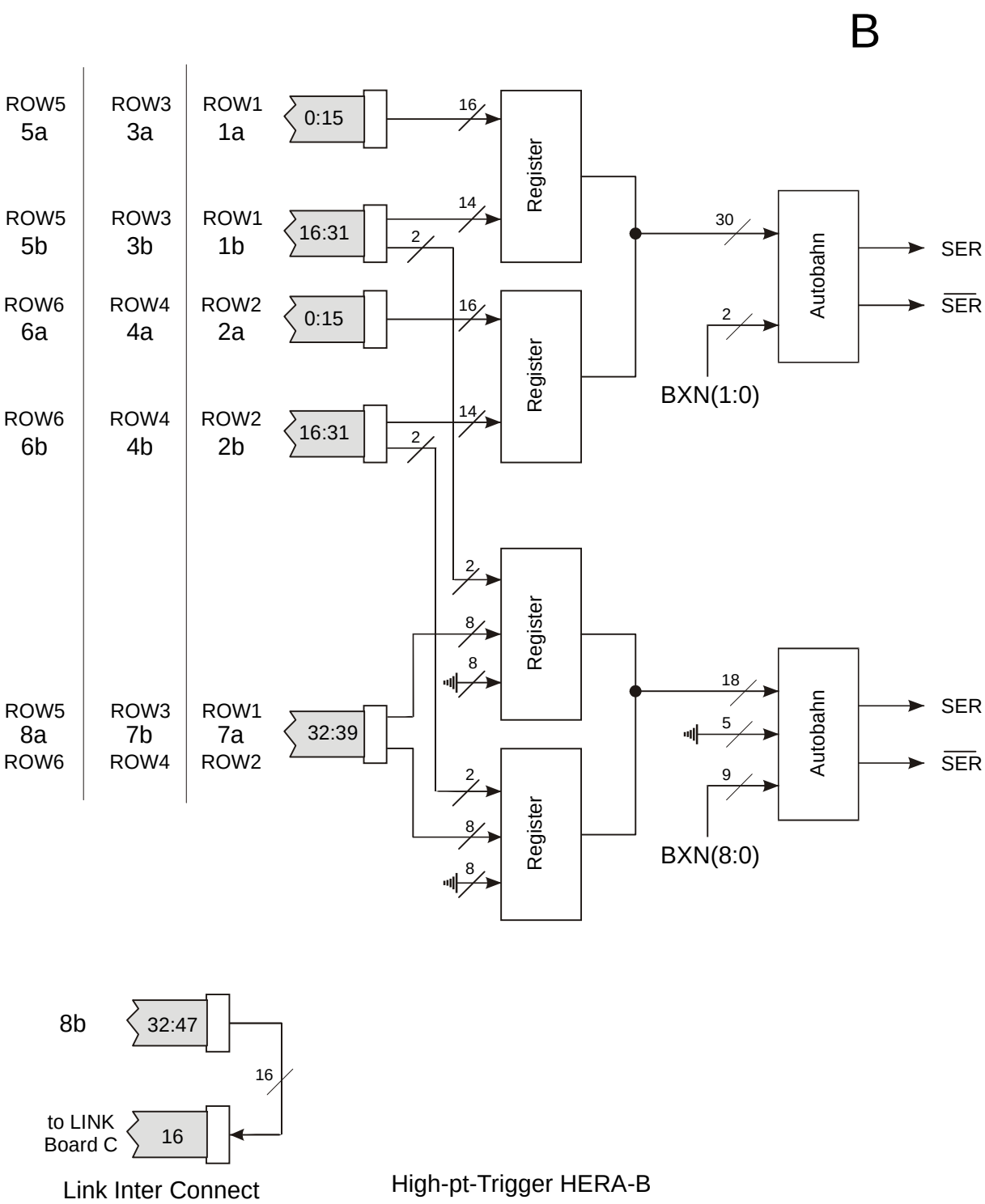


High-pt-Trigger HERA-B

LINK-BOARD A

1 out of 4 link channels shown

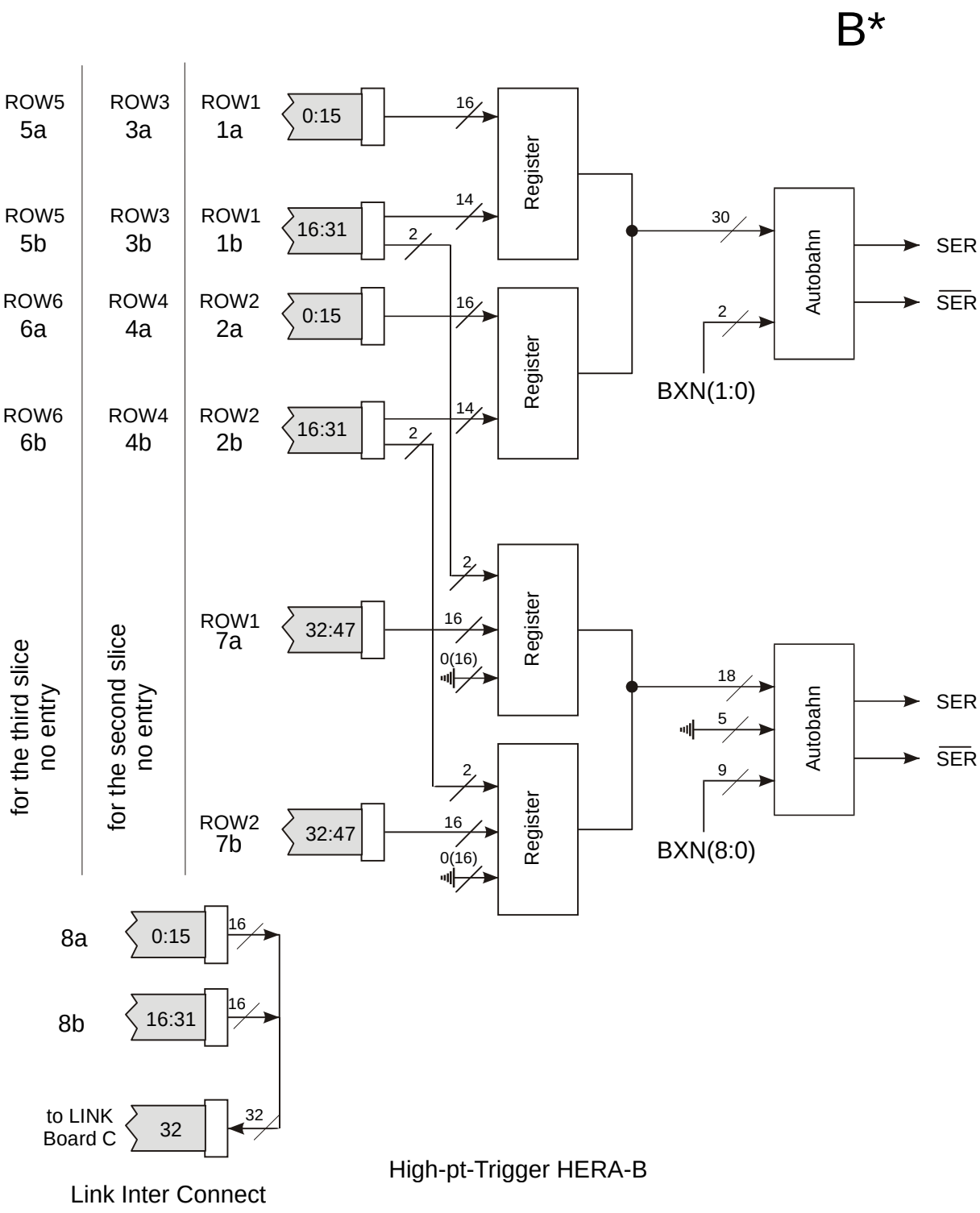
4) Logic Diagram of Link Board B



LINK- BOARD B

1 out of 3 link channels shown

5) Logic Diagram of Link Board B*

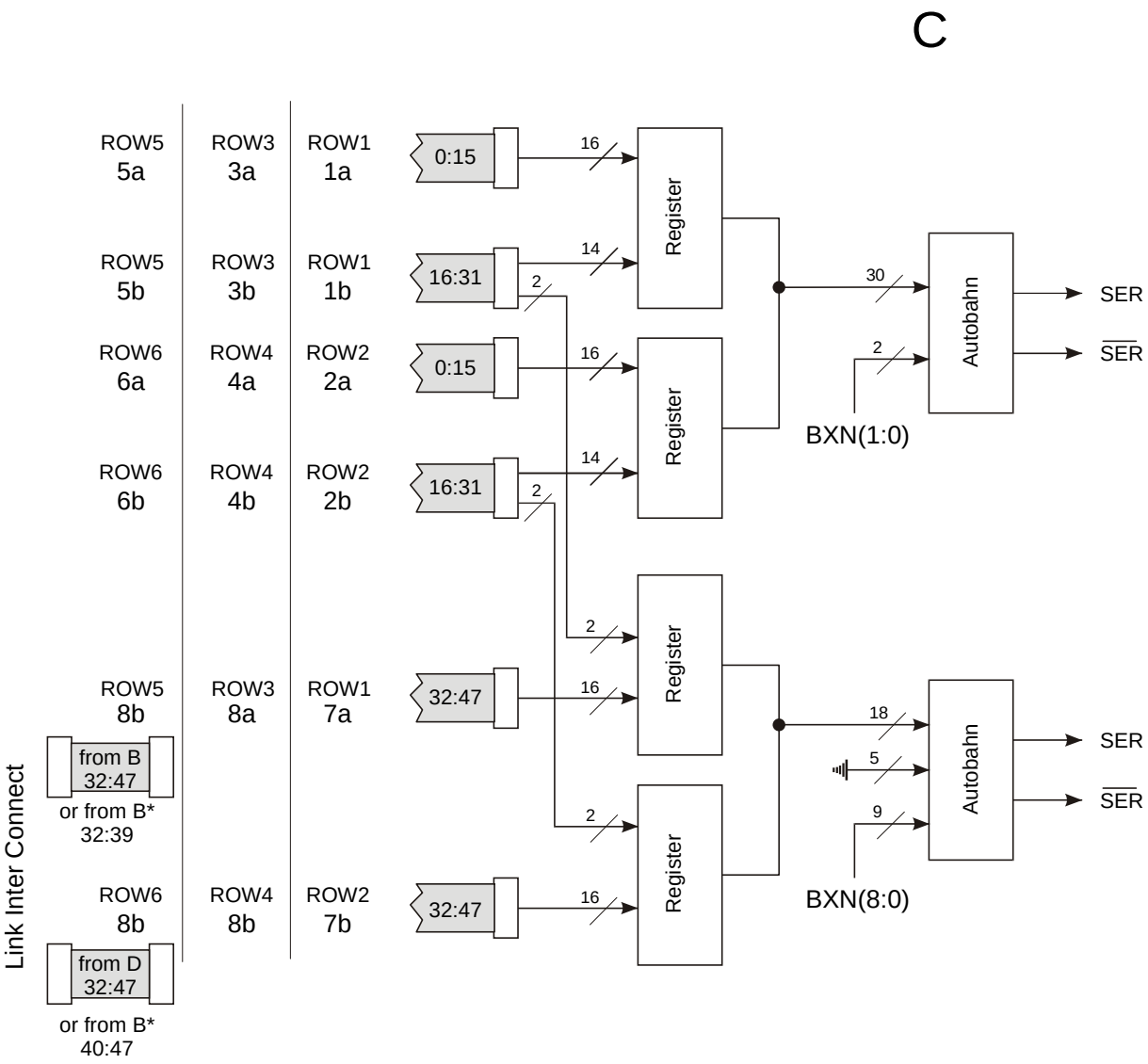


High-pt-Trigger HERA-B

LINK- BOARD B*

1 out of 3 link channels shown

6) Logic Diagram of Link Board C

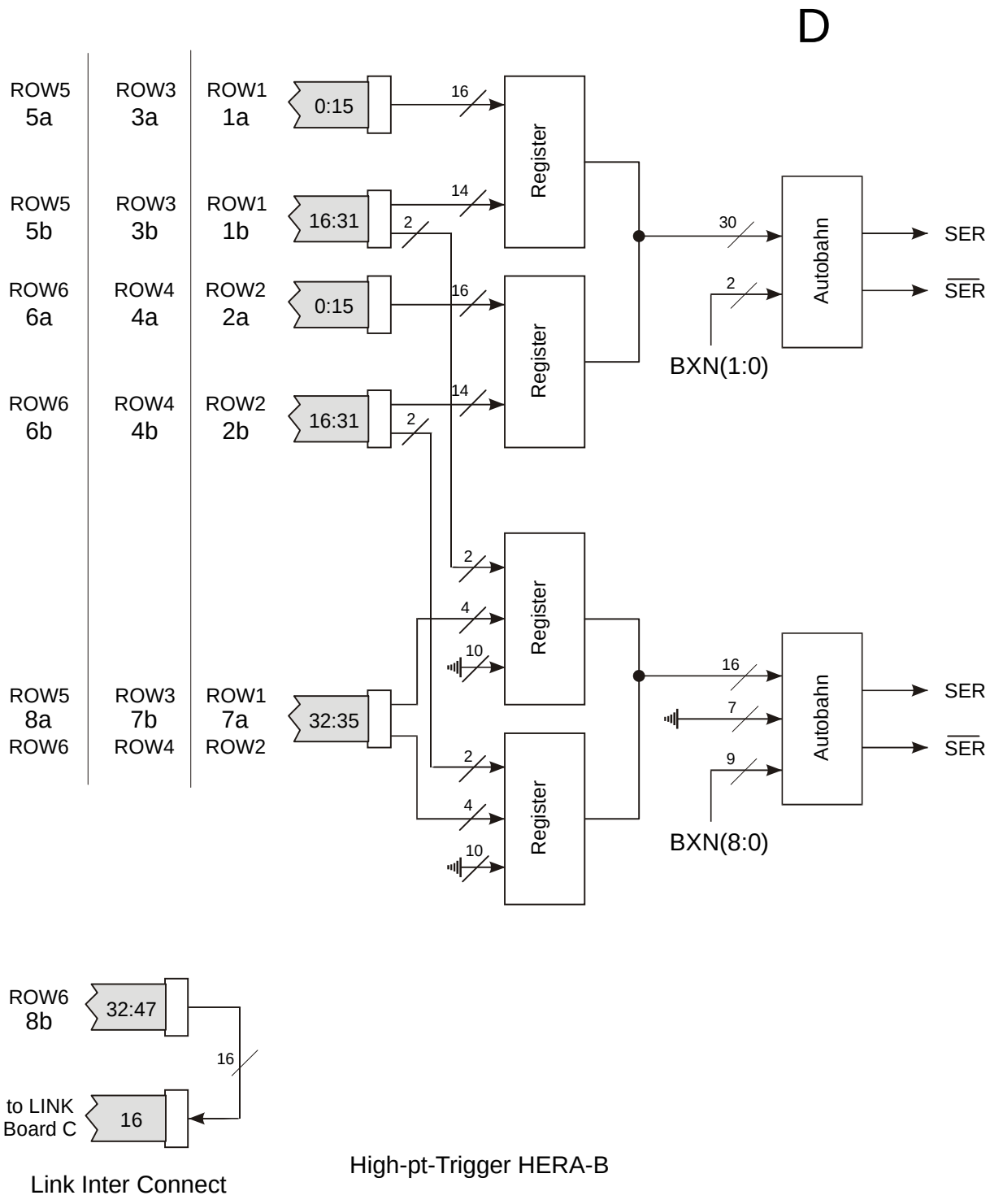


High-pt-Trigger HERA-B

LINK-BOARD C

1 out of 3 link channels shown

7) Logic Diagram of Link Board D



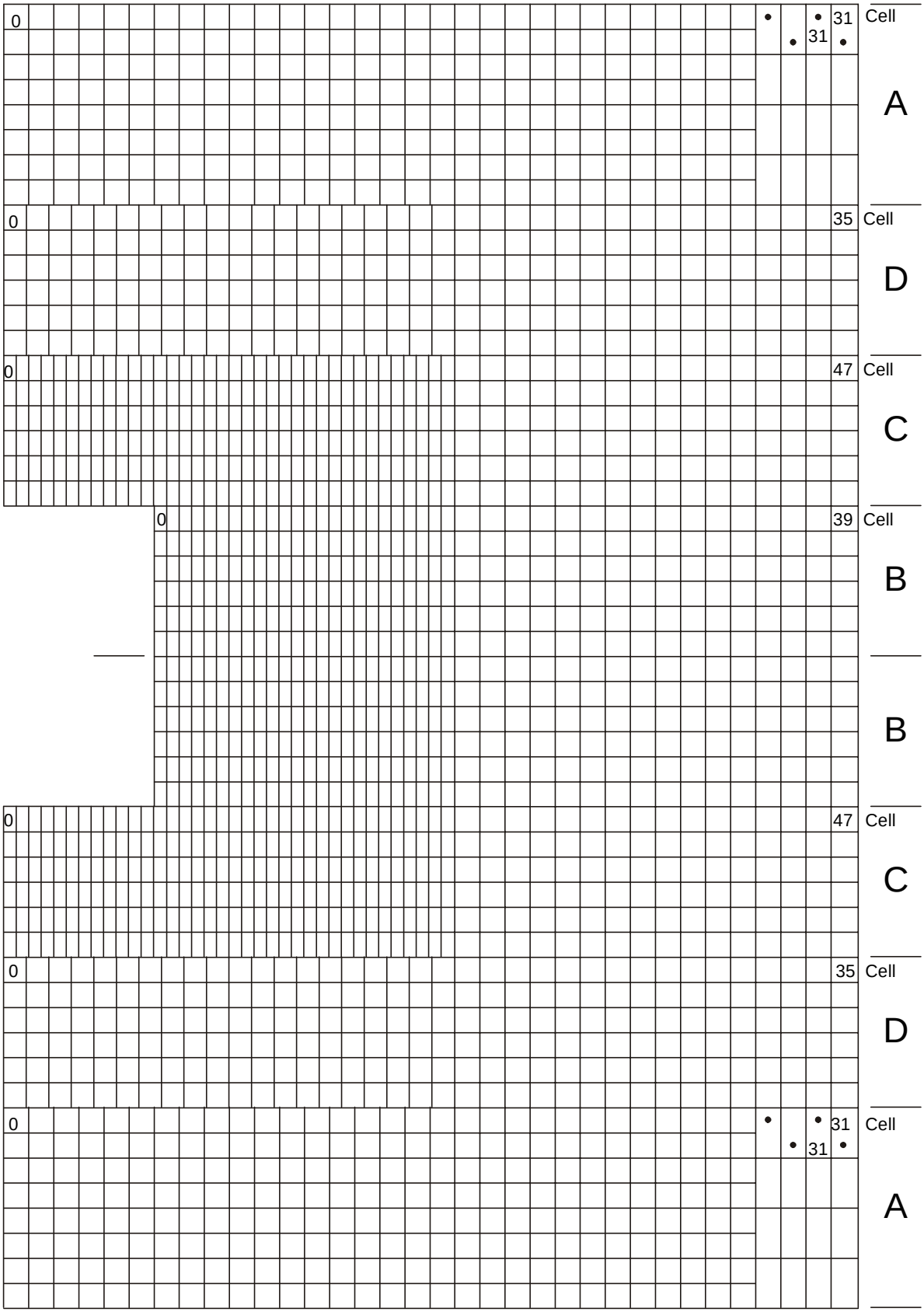
Link Inter Connect

High-pt-Trigger HERA-B

LINK-BOARD D

1 out of 3 link channels shown

8) Sections of inner Detector



the cell sizes are not to scale!

HERA B

high Pt inner chamber

9) Pixel Allocation of inner Detector

Detector		FED		Link Board			2. Link Board		
Row	**Pixel**	**Num.**	**Con.**	**Num.**	**Type**	**Output**	**Num.**	**Type**	**Output**
1	0..15	1	1a	1	A	Channel 1			
1	16..31	1	1b	1	A	Channel 1			
2	0..15	1	2a	1	A	Channel 1			
2	16..31	1	2b	1	A	Channel 1			
3	0..15	1	3a	1	A	Channel 2			
3	16..31	1	3b	1	A	Channel 2			
4	0..15	1	4a	1	A	Channel 2			
4	16..31	1	4b	1	A	Channel 2			
5	0..15	1	5a	1	A	Channel 3			
5	16..31	1	5b	1	A	Channel 3			
6	0..15	1	6a	1	A	Channel 3			
6	16..31	1	6b	1	A	Channel 3			
7	0..15	1	7a	1	A	Channel 4			
7	16..31	1	7b	1	A	Channel 4			
8	0..15	1	8a	1	A	Channel 4			
8	16..31	1	8b	1	A	Channel 4			
9	0..15	2	1a	2	D	Channel 1			
9	16..31	2	1b	2	D	Channel 1			
9	32..35	2	7a	2	D	Channel 1			
10	0..15	2	2a	2	D	Channel 1			
10	16..31	2	2b	2	D	Channel 1			
10	32..35	2	7a	2	D	Channel 1			
11	0..15	2	3a	2	D	Channel 2			
11	16..31	2	3b	2	D	Channel 2			
11	32..35	2	7b	2	D	Channel 2			
12	0..15	2	4a	2	D	Channel 2			
12	16..31	2	4b	2	D	Channel 2			
12	32..35	2	7b	2	D	Channel 2			
13	0..15	2	5a	2	D	Channel 3			
13	16..31	2	5b	2	D	Channel 3			
13	32..35	2	8a	2	D	Channel 3			
14	0..15	2	6a	2	D	Channel 3			
14	16..31	2	6b	2	D	Channel 3			
14	32..35	2	8a	2	D	Channel 3			
15	0..15	3	1a	3	C	Channel 1			
15	16..31	3	1b	3	C	Channel 1			
15	32..47	3	7a	3	C	Channel 1			
16	0..15	3	2a	3	C	Channel 1			
16	16..31	3	2b	3	C	Channel 1			
16	32..47	3	7b	3	C	Channel 1			
17	0..15	3	3a	3	C	Channel 2			
17	16..31	3	3b	3	C	Channel 2			
17	32..47	3	8a	3	C	Channel 2			
18	0..15	3	4a	3	C	Channel 2			
18	16..31	3	4b	3	C	Channel 2			
18	32..47	3	8b	3	C	Channel 2			
19	0..15	3	5a	3	C	Channel 3			
19	16..31	3	5b	3	C	Channel 3			
19	32..47	2	8b	2	D	LIC	3	C	Channel 3
20	0..15	3	6a	3	C	Channel 3			
20	16..31	3	6b	3	C	Channel 3			
20	32..47	4	8b	4	B	LIC	3	C	Channel 3

Detector		FED		Link Board			2. Link Board		
Row	**Pixel**	**Num.**	**Con.**	**Num.**	**Type**	**Output**	**Num.**	**Type**	**Output**
21	0..15	4	1a	4	B	Channel 1			
21	16..31	4	1b	4	B	Channel 1			
21	32..39	4	7a	4	B	Channel 1			
22	0..15	4	2a	4	B	Channel 1			
22	16..31	4	2b	4	B	Channel 1			
22	32..39	4	7a	4	B	Channel 1			
23	0..15	4	3a	4	B	Channel 2			
23	16..31	4	3b	4	B	Channel 2			
23	32..39	4	7b	4	B	Channel 2			
24	0..15	4	4a	4	B	Channel 2			
24	16..31	4	4b	4	B	Channel 2			
24	32..39	4	7b	4	B	Channel 2			
25	0..15	4	5a	4	B	Channel 3			
25	16..31	4	5b	4	B	Channel 3			
25	32..39	4	8a	4	B	Channel 3			
26	0..15	4	6a	4	B	Channel 3			
26	16..31	4	6b	4	B	Channel 3			
26	32..39	4	8a	4	B	Channel 3			
27	0..15	5	1a	5	B	Channel 1			
27	16..31	5	1b	5	B	Channel 1			
27	32..39	5	7a	5	B	Channel 1			
28	0..15	5	2a	5	B	Channel 1			
28	16..31	5	2b	5	B	Channel 1			
28	32..39	5	7a	5	B	Channel 1			
29	0..15	5	3a	5	B	Channel 2			
29	16..31	5	3b	5	B	Channel 2			
29	32..39	5	7b	5	B	Channel 2			
30	0..15	5	4a	5	B	Channel 2			
30	16..31	5	4b	5	B	Channel 2			
30	32..39	5	7b	5	B	Channel 2			
31	0..15	5	5a	5	B	Channel 3			
31	16..31	5	5b	5	B	Channel 3			
31	32..39	5	8a	5	B	Channel 3			
32	0..15	5	6a	5	B	Channel 3			
32	16..31	5	6b	5	B	Channel 3			
32	32..39	5	8a	5	B	Channel 3			
33	0..15	6	1a	6	C	Channel 1			
33	16..31	6	1b	6	C	Channel 1			
33	32..47	6	7a	6	C	Channel 1			
34	0..15	6	2a	6	C	Channel 1			
34	16..31	6	2b	6	C	Channel 1			
34	32..47	6	7b	6	C	Channel 1			
35	0..15	6	3a	6	C	Channel 2			
35	16..31	6	3b	6	C	Channel 2			
35	32..47	6	8a	6	C	Channel 2			
36	0..15	6	4a	6	C	Channel 2			
36	16..31	6	4b	6	C	Channel 2			
36	32..47	6	8b	6	C	Channel 2			
37	0..15	6	5a	6	C	Channel 3			
37	16..31	6	5b	6	C	Channel 3			
37	32..47	5	8b	5	B	LIC	6	C	Channel 3
38	0..15	6	6a	6	C	Channel 3			
38	16..31	6	6b	6	C	Channel 3			
38	32..47	7	8b	7	D	LIC	6	C	Channel 3

Detector		FED		Link Board			2. Link Board		
Row	**Pixel**	**Num.**	**Con.**	**Num.**	**Type**	**Output**	**Num.**	**Type**	**Output**
39	0..15	7	1a	7	D	Channel 1			
39	16..31	7	1b	7	D	Channel 1			
39	32..35	7	7a	7	D	Channel 1			
40	0..15	7	2a	7	D	Channel 1			
40	16..31	7	2b	7	D	Channel 1			
40	32..35	7	7a	7	D	Channel 1			
41	0..15	7	3a	7	D	Channel 2			
41	16..31	7	3b	7	D	Channel 2			
41	32..35	7	7b	7	D	Channel 2			
42	0..15	7	4a	7	D	Channel 2			
42	16..31	7	4b	7	D	Channel 2			
42	32..35	7	7b	7	D	Channel 2			
43	0..15	7	5a	7	D	Channel 3			
43	16..31	7	5b	7	D	Channel 3			
43	32..35	7	8a	7	D	Channel 3			
44	0..15	7	6a	7	D	Channel 3			
44	16..31	7	6b	7	D	Channel 3			
44	32..35	7	8a	7	D	Channel 3			
45	0..15	8	1a	8	A	Channel 1			
45	16..31	8	1b	8	A	Channel 1			
46	0..15	8	2a	8	A	Channel 1			
46	16..31	8	2b	8	A	Channel 1			
47	0..15	8	3a	8	A	Channel 2			
47	16..31	8	3b	8	A	Channel 2			
48	0..15	8	4a	8	A	Channel 2			
48	16..31	8	4b	8	A	Channel 2			
49	0..15	8	5a	8	A	Channel 3			
49	16..31	8	5b	8	A	Channel 3			
50	0..15	8	6a	8	A	Channel 3			
50	16..31	8	6b	8	A	Channel 3			
51	0..15	8	7a	8	A	Channel 4			
51	16..31	8	7b	8	A	Channel 4			
52	0..15	8	8a	8	A	Channel 4			
52	16..31	8	8b	8	A	Channel 4			

10) Sections of outer Detector (left Side +x)

C_1	1	LIC from D_2, 8b		6b	6a
	2	LIC from D_1, 8b		5b	5a
	3	8b		4b	4a
	4	8a		3b	3a
	5	7b		2b	2a
	6	7a		1b	1a
C_2	7	7b		2b	2a
	8	7a		1b	1a
D_1	9	8a	6b	6a	
	10	8a	5b	5a	
	11	7b	4b	4a	
	12	7b	3b	3a	
	13	7a	2b	2a	
	14	7a	1b	1a	
D_2	15	7a	1b	1a	
	16	7a	2b	2a	
	17	7b	3b	3a	
	18	7b	4b	4a	
	19	8a	5b	5a	
	20	8a	6b	6a	
C_2	21	8a		3b	3a
	22	8b		4b	4a
C_3	L1-23	7a		1b	1a
	L2-23	8a		3b	3a
C_4	L3-23	7a		1b	1a

This figure also shows schematically the required connection of detector pads to FED input connectors, which is given in more detail in the following table.
Link Board C_3 covers detector row #23 of the first two layers.
Link Board C_4 covers detector row #23 of the third layer.

11) Pixel Allocation of outer Detector (left Side +x)

Detector		FED		Link Board			2. Link Board		
Row	**Pixel**	**Num.**	**Con.**	**Num.**	**Type**	**Output**	**Num.**	**Type**	**Output**
1	0..15	2	6a	2	C	Channel 3			
1	16..31	2	6b	2	C	Channel 3			
1	32..47	3	8b	3	D	LIC	2	C	Channel 3
2	0..15	2	5a	2	C	Channel 3			
2	16..31	2	5b	2	C	Channel 3			
2	32..47	1	8b	1	D	LIC	2	C	Channel 3
3	0..15	2	4a	2	C	Channel 2			
3	16..31	2	4b	2	C	Channel 2			
3	32..47	2	8b	2	C	Channel 2			
4	0..15	2	3a	2	C	Channel 2			
4	16..31	2	3b	2	C	Channel 2			
4	32..47	2	8a	2	C	Channel 2			
5	0..15	2	2a	2	C	Channel 1			
5	16..31	2	2b	2	C	Channel 1			
5	32..47	2	7b	2	C	Channel 1			
6	0..15	2	1a	2	C	Channel 1			
6	16..31	2	1b	2	C	Channel 1			
6	32..47	2	7a	2	C	Channel 1			
7	0..15	4	2a	4	C	Channel 1			
7	16..31	4	2b	4	C	Channel 1			
7	32..47	4	7b	4	C	Channel 1			
8	0..15	4	1a	4	C	Channel 1			
8	16..31	4	1b	4	C	Channel 1			
8	32..47	4	7a	4	C	Channel 1			
9	0..15	1	6a	1	D	Channel 3			
9	16..31	1	6b	1	D	Channel 3			
9	32..35	1	8a	1	D	Channel 3			
10	0..15	1	5a	1	D	Channel 3			
10	16..31	1	5b	1	D	Channel 3			
10	32..35	1	8a	1	D	Channel 3			
11	0..15	1	4a	1	D	Channel 2			
11	16..31	1	4b	1	D	Channel 2			
11	32..35	1	7b	1	D	Channel 2			
12	0..15	1	3a	1	D	Channel 2			
12	16..31	1	3b	1	D	Channel 2			
12	32..35	1	7b	1	D	Channel 2			
13	0..15	1	2a	1	D	Channel 1			
13	16..31	1	2b	1	D	Channel 1			
13	32..35	1	7a	1	D	Channel 1			
14	0..15	1	1a	1	D	Channel 1			
14	16..31	1	1b	1	D	Channel 1			
14	32..35	1	7a	1	D	Channel 1			

Detector		FED		Link Board			2. Link Board		
Row	**Pixel**	**Num.**	**Con.**	**Num.**	**Type**	**Output**	**Num.**	**Type**	**Output**
15	0..15	3	1a	3	D	Channel 1			
15	16..31	3	1b	3	D	Channel 1			
15	32..35	3	7a	3	D	Channel 1			
16	0..15	3	2a	3	D	Channel 1			
16	16..31	3	2b	3	D	Channel 1			
16	32..35	3	7a	3	D	Channel 1			
17	0..15	3	3a	3	D	Channel 2			
17	16..31	3	3b	3	D	Channel 2			
17	32..35	3	7b	3	D	Channel 2			
18	0..15	3	4a	3	D	Channel 2			
18	16..31	3	4b	3	D	Channel 2			
18	32..35	3	7b	3	D	Channel 2			
19	0..15	3	5a	3	D	Channel 3			
19	16..31	3	5b	3	D	Channel 3			
19	32..35	3	8a	3	D	Channel 3			
20	0..15	3	6a	3	D	Channel 3			
20	16..31	3	6b	3	D	Channel 3			
20	32..35	3	8a	3	D	Channel 3			
21	0..15	4	3a	4	C	Channel 2			
21	16..31	4	3b	4	C	Channel 2			
21	32..47	4	8a	4	C	Channel 2			
22	0..15	4	4a	4	C	Channel 2			
22	16..31	4	4b	4	C	Channel 2			
22	32..47	4	8b	4	C	Channel 2			
L1-23	0..15	5	1a	5	C	Channel 1			
L1-23	16..31	5	1b	5	C	Channel 1			
L1-23	32..47	5	7a	5	C	Channel 1			
L2-23	0..15	5	3a	5	C	Channel 2			
L2-23	16..31	5	3b	5	C	Channel 2			
L2-23	32..47	5	8a	5	C	Channel 2			
L3-23	0..15	6	1a	6	C	Channel 1			
L3-23	16..31	6	1b	6	C	Channel 1			
L3-23	32..47	6	7a	6	C	Channel 1			

12) Sections of outer Detector (right Side -x)

6a	6b	---		1	C_1
5a	5b	LIC from D_1, 8b		2	
4a	4b	8b		3	
3a	3b	8a		4	
2a	2b	7b		5	
1a	1b	7a		6	
2a	2b	7b		7	C_3
1a	1b	7a		8	
6a	6b		8a	9	D_1
5a	5b		8a	10	
4a	4b		7b	11	
3a	3b		7b	12	
2a	2b		7a	13	
1a	1b		7a	14	
1a	1b		7a	15	D_2
2a	2b		7a	16	
3a	3b		7b	17	
4a	4b		7b	18	
5a	5b		8a	19	
6a	6b		8a	20	
3a	3b	8a		21	C_3
4a	4b	8b		22	
1a	1b	7a		23	C_2
2a	2b	7b		24	
3a	3b	8a		25	
4a	4b	8b		26	
5a	5b	LIC from D_2, 8b		27	
6a	6b	---		28	

This figure also shows schematically the required connection of detector pads to FED input connectors, which is given in more detail in the following table.

13) Pixel Allocation of outer Detector (right Side -x)

Detector		FED		Link Board			2. Link Board		
Row	**Pixel**	**Num.**	**Con.**	**Num.**	**Type**	**Output**	**Num.**	**Type**	**Output**
1	0..15	2	6a	2	C	Channel 3			
1	16..31	2	6b	2	C	Channel 3			
1	32..47	-	-	-	-	-			
2	0..15	2	5a	2	C	Channel 3			
2	16..31	2	5b	2	C	Channel 3			
2	32..47	1	8b	1	D	LIC	2	C	Channel 3
3	0..15	2	4a	2	C	Channel 2			
3	16..31	2	4b	2	C	Channel 2			
3	32..47	2	8b	2	C	Channel 2			
4	0..15	2	3a	2	C	Channel 2			
4	16..31	2	3b	2	C	Channel 2			
4	32..47	2	8a	2	C	Channel 2			
5	0..15	2	2a	2	C	Channel 1			
5	16..31	2	2b	2	C	Channel 1			
5	32..47	2	7b	2	C	Channel 1			
6	0..15	2	1a	2	C	Channel 1			
6	16..31	2	1b	2	C	Channel 1			
6	32..47	2	7a	2	C	Channel 1			
7	0..15	5	2a	5	C	Channel 1			
7	16..31	5	2b	5	C	Channel 1			
7	32..47	5	7b	5	C	Channel 1			
8	0..15	5	1a	5	C	Channel 1			
8	16..31	5	1b	5	C	Channel 1			
8	32..47	5	7a	5	C	Channel 1			
9	0..15	1	6a	1	D	Channel 3			
9	16..31	1	6b	1	D	Channel 3			
9	32..35	1	8a	1	D	Channel 3			
10	0..15	1	5a	1	D	Channel 3			
10	16..31	1	5b	1	D	Channel 3			
10	32..35	1	8a	1	D	Channel 3			
11	0..15	1	4a	1	D	Channel 2			
11	16..31	1	4b	1	D	Channel 2			
11	32..35	1	7b	1	D	Channel 2			
12	0..15	1	3a	1	D	Channel 2			
12	16..31	1	3b	1	D	Channel 2			
12	32..35	1	7b	1	D	Channel 2			
13	0..15	1	2a	1	D	Channel 1			
13	16..31	1	2b	1	D	Channel 1			
13	32..35	1	7a	1	D	Channel 1			
14	0..15	1	1a	1	D	Channel 1			
14	16..31	1	1b	1	D	Channel 1			
14	32..35	1	7a	1	D	Channel 1			

Detector		FED		Link Board			2. Link Board		
Row	**Pixel**	**Num.**	**Con.**	**Num.**	**Type**	**Output**	**Num.**	**Type**	**Output**
15	0..15	3	1a	3	D	Channel 1			
15	16..31	3	1b	3	D	Channel 1			
15	32..35	3	7a	3	D	Channel 1			
16	0..15	3	2a	3	D	Channel 1			
16	16..31	3	2b	3	D	Channel 1			
16	32..35	3	7a	3	D	Channel 1			
17	0..15	3	3a	3	D	Channel 2			
17	16..31	3	3b	3	D	Channel 2			
17	32..35	3	7b	3	D	Channel 2			
18	0..15	3	4a	3	D	Channel 2			
18	16..31	3	4b	3	D	Channel 2			
18	32..35	3	7b	3	D	Channel 2			
19	0..15	3	5a	3	D	Channel 3			
19	16..31	3	5b	3	D	Channel 3			
19	32..35	3	8a	3	D	Channel 3			
20	0..15	3	6a	3	D	Channel 3			
20	16..31	3	6b	3	D	Channel 3			
20	32..35	3	8a	3	D	Channel 3			
21	0..15	5	3a	5	C	Channel 2			
21	16..31	5	3b	5	C	Channel 2			
21	32..47	5	8a	5	C	Channel 2			
22	0..15	5	4a	5	C	Channel 2			
22	16..31	5	4b	5	C	Channel 2			
22	32..47	5	8b	5	C	Channel 2			
23	0..15	4	1a	4	C	Channel 1			
23	16..31	4	1b	4	C	Channel 1			
23	32..47	4	7a	4	C	Channel 1			
24	0..15	4	2a	4	C	Channel 1			
24	16..31	4	2b	4	C	Channel 1			
24	32..47	4	7b	4	C	Channel 1			
25	0..15	4	3a	4	C	Channel 2			
25	16..31	4	3b	4	C	Channel 2			
25	32..47	4	8a	4	C	Channel 2			
26	0..15	4	4a	4	C	Channel 2			
26	16..31	4	4b	4	C	Channel 2			
26	32..47	4	8b	4	C	Channel 2			
27	0..15	4	5a	4	C	Channel 3			
27	16..31	4	5b	4	C	Channel 3			
27	32..47	3	8b	3	D	LIC	4	C	Channel 3
28	0..15	4	6a	4	C	Channel 3			
28	16..31	4	6b	4	C	Channel 3			
28	32..47	-	-	-	-	-			