VFPS Electronics

Manual

Preliminary

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Contents

I. Introduction

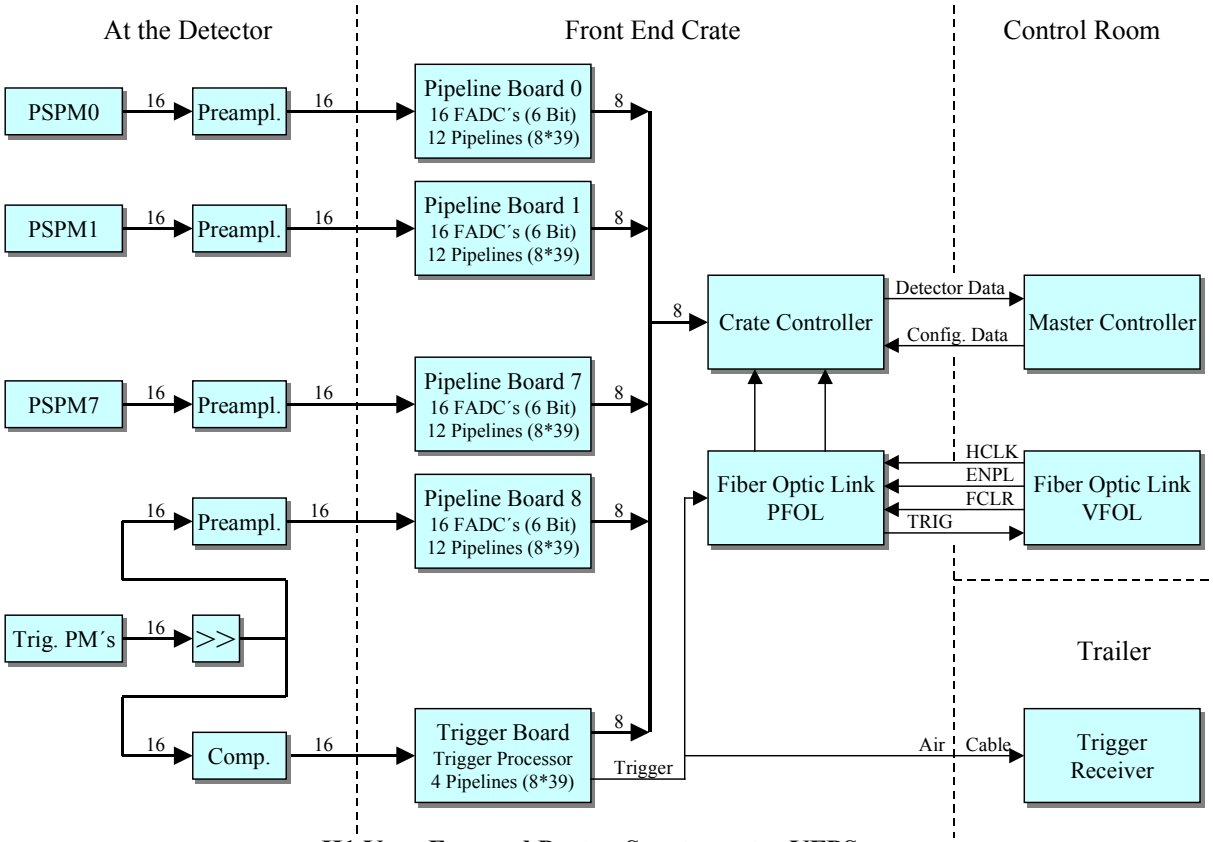
This manual describes the electronics for one Roman Pot of the H1 Very Forward Proton Spectrometer VFPS. At first a more general overview of the complete equipment is given. The following chapter provides all information necessary to program and operate the system. Finally some recommendations are given for first test and data acquisition runs.

II. Electronics Overview

The electronics of the H1 Very Forward Proton Spectrometer mainly can be subdivided into three parts:

- The front end components, consisting of preamplifiers and comparators, are mounted directly on the detector.
- The conversion and pipelining electronics are located a few meters apart from the detector in the Front End Crate.
- The Master Controller, providing experiment control and data read out, is a VME module, residing in a STC crate in Control Room 101 together with a fiber optic link module for control signal transmission.

These parts are shown in the following block diagram. The detector is equipped with 8 PSPM´s of 16 pixels each (Hamamatsu H6568). The resulting 128 analog signals are processed at first by charge sensitive preamplifiers with differential outputs in order to be able to drive the outgoing pulses to the external Front End Crate with sufficient common mode rejection.



H1 Very Forward Proton Spectrometer VFPS

Readout Scheme for one Pot

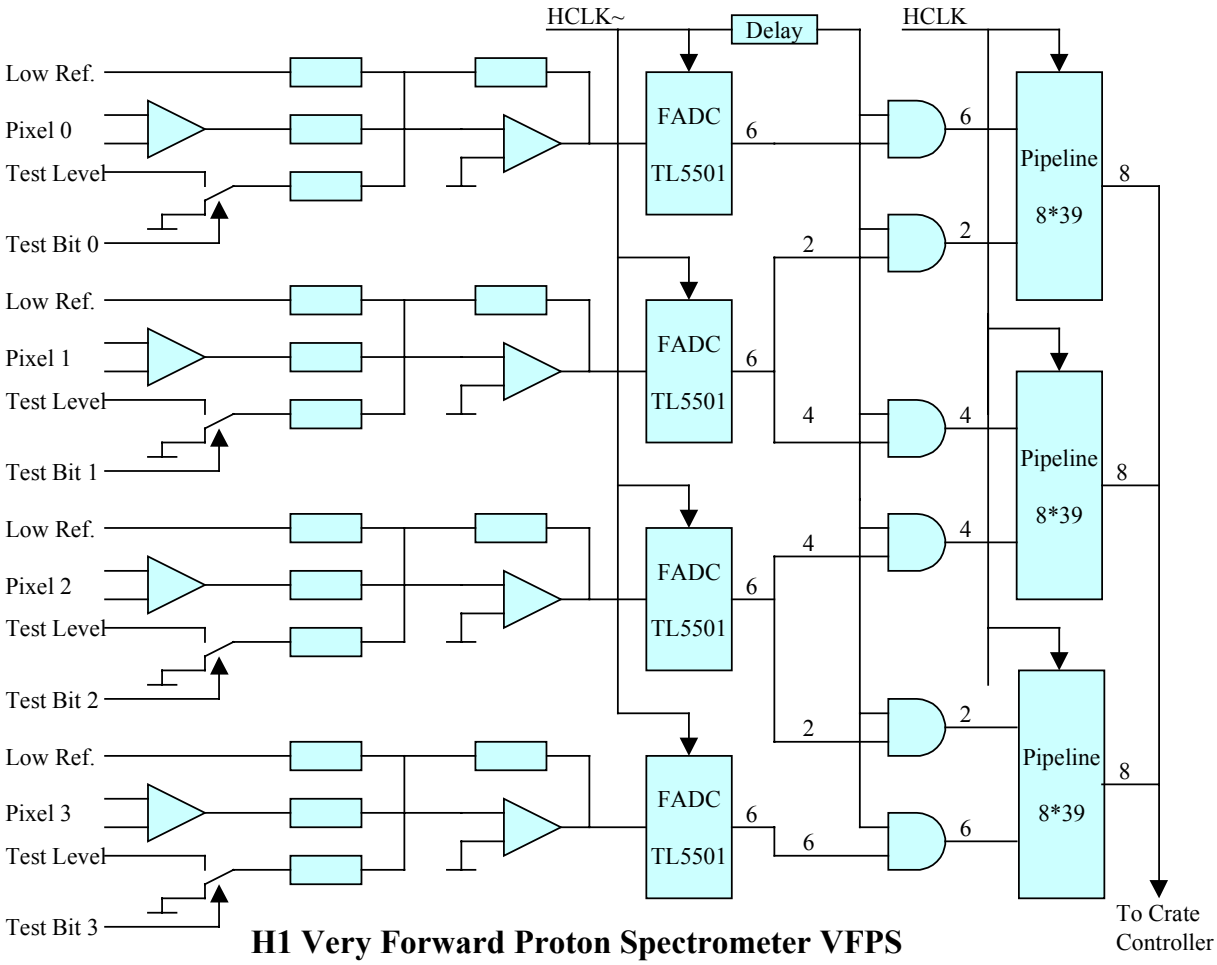
Here the analog pixel informations are distributed to 8 Pipeline Boards of 16 channels each, where they are converted by 6 bit FADC´s. On each board the resulting 96 bits are issued to 12 pipelines of 8 bits width and 39 stages depth each. The pipeline output registers are addressed by a 9 bit address bus and read out via an 8 bit data bus on the crate backplane.
Additionally each event provides 16 signals of the tile trigger detector photomultipliers (Hamamatsu R7400U). They are converted to digital pulses by fast comparators with remote controlled threshold. The resulting hit pattern is transferred to the Trigger Board, where it is stored in a pipeline and used as input to the Trigger Processor, which checks the implemented trigger conditions and generates the Trigger signal.
Furthermore the 16 trigger tile signals are processed also by the FADC´s of an additional Pipeline Board. So in case of a trigger, 128*6 bits = 96 bytes of pixel FADC data, 16*6 bits = 12 bytes of trigger FADC data and 4 bytes of Trigger Board informations have to be read out by the Crate Controller. It is connected to the Master Controller in the Control Room by means of a pair of optical fibers, one for transmission of detector data and one for sending configuration data to the front end.
There is another Fiber Optic Link, on which the unit **VFOL** in the STC Crate transmits the control signals **HCLK** (H1 System Clock), **ENPL** (Enable Pipeline) and **FCLR** (Fast Clear) to the unit **PFOL** in the Front End Crate and receives the trigger signal **TRIG**, which is used for local mode operation (data acquisition without HERA Central Trigger).
For data acquisition in normal mode the trigger signal is send directly to the H1 Central Trigger System via a special Air Cable (propagation delay < 4 nsec/m) in order to provide the signal in time for the first level trigger.

1) Front End Electronics

Assuming a mean yield of 5 photoelectrons per fiber and a PSMP amplification factor of $3*10^6$, one can expect at the PSPM anode an average charge signal of about 2.5 pC. Therefore a charge sensitive preamplifier with a sensitivity of the order of 100 mV/pC has been foreseen as first step in the signal processing chain, followed by a differential driver circuit, which is capable to drive the signals via twisted pair cables to the external Front End Crate. Since one Preamplifier Board contains 32 channels, one needs 4 boards for one Roman Pot.
The Comparator Board has been designed for the FPS detector and provides 8 comparators with negative threshold and 4 comparators with positive threshold. For the VFPS application only the first ones are used. Therefore two boards are required for one Roman Pot. The threshold is common for all comparators and can be set by remote programming an 8 bit DAC on the Crate Controller.

2) Pipeline Board

The Pipeline Board, a quarter of which is shown in the following block diagram, has been designed to convert and pipeline the informations of 16 PSPM signals.



H1 Very Forward Proton Spectrometer VFPS

Pipeline Board (4 of 16 Channels)

The main purpose of the operational amplifier at the FADC input is to sum the following three signal sources:

- The analog pixel information coming from the differential receiver.
- A constant voltage ‘Low Ref.’, which shifts the signal level to the sensitive range of the FADC.
- A test level, which optionally can be added by setting the appropriate Test Bit, in order to be able to test the response of the complete read-out chain on a known input level. It represents approximately the half of the conversion range.

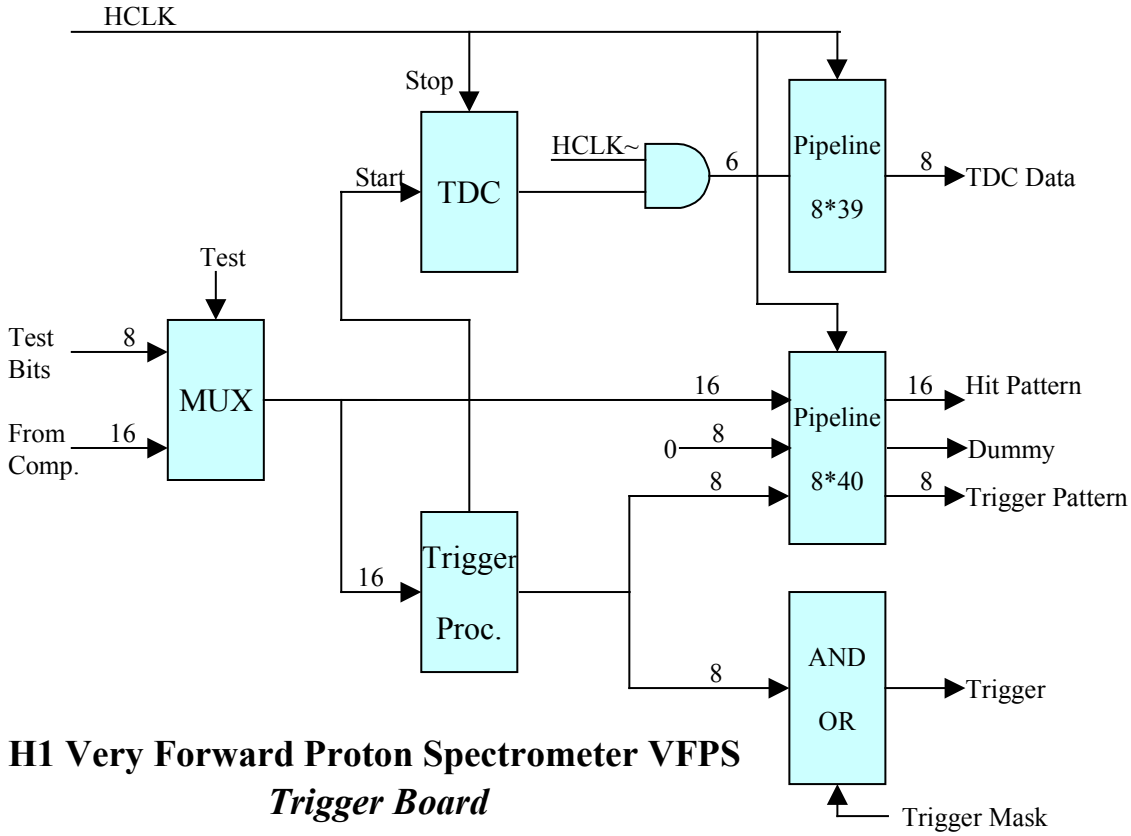
The FADC of type TL5501 (Texas Instruments) has an input range of 1 Volt, a resolution of 6 bits and a maximum conversion rate of 30 MHz. In this application it is clocked by the H1 clock, providing the conversion result 96 nsec after conversion start. So the FADC acts as the first stage of the event pipeline.

The FADC output levels are gated in order to force all bits to zero between two events. That is required by the input stage of the following pipeline device. As shown in the block diagram the 24 bits of 4 FADC´s are distributed to 3 pipeline registers of 8 bit width each, in order to save board space and money.

As pipeline device a special cost effective and high integrated ASIC chip is used, which has been developed for the H1 Streamer Tube Detector [1] and has a depth of 32 stages. Since that number is not sufficient for the VFPS, which is located more than 200 m apart from the interaction point, the pipeline depth has been enlarged to 39 stages by adding CPLD´s (Altera EPM7064S), where 8*9 pipeline registers are implemented by in system programmable firmware.
Each pipeline output register can be addressed individually via an address bus on the backplane. For reasons of data integrity the read-out of the board address is additionally provided. So the complete address space of one Pipeline Board is 13 bytes.

3) Trigger Board

The Trigger Board processes 16 digital signals coming from the comparators of the trigger tile detectors. For test purposes 8 test bits are foreseen, each one emulating two input signals simultaneously.



H1 Very Forward Proton Spectrometer VFPS
Trigger Board

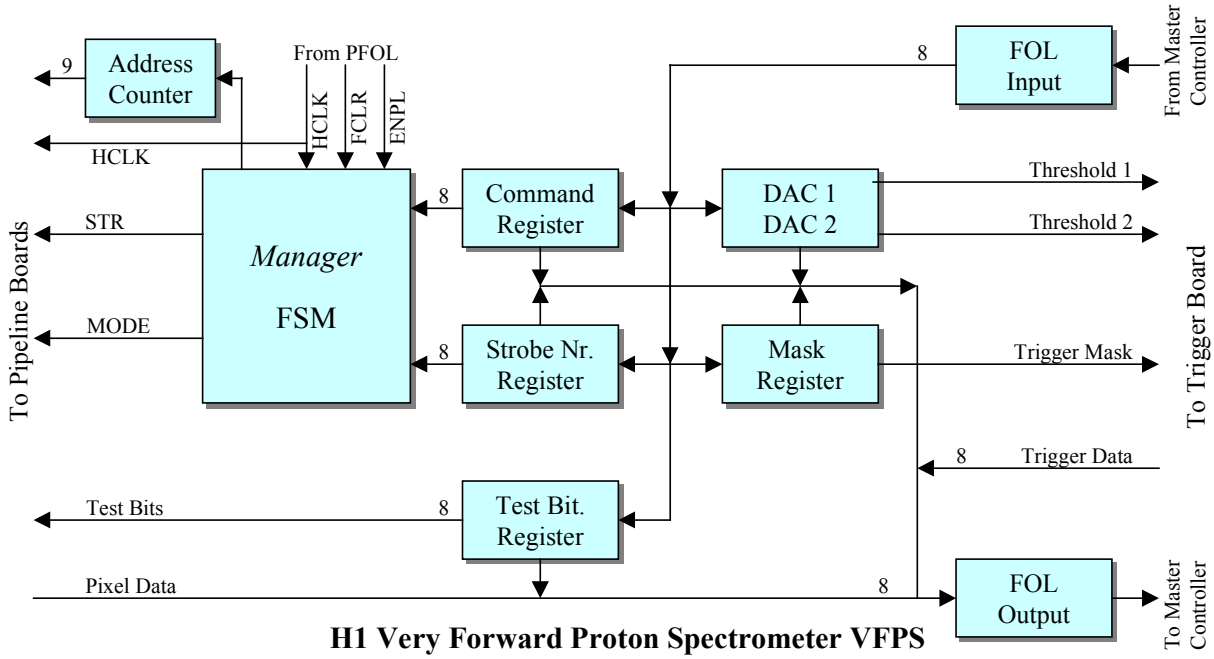
The input lines are connected to the Hit Pattern pipeline and additionally to the Trigger Processor, where 8 different trigger conditions, implemented by firmware, are checked. That procedure needs only 20 nsec, so that the resulting Trigger Pattern of 8 bits, where each bit represents one trigger condition, can be stored together with the corresponding Hit Pattern in the pipeline by the next active clock transition.
The eight trigger conditions can be activated by means of 8 bits of the Trigger Mask, which is remote programmable. The final trigger signal then is the logical OR of the masked Trigger Pattern.
Additionally a facility is provided to measure the time, at which the first of the programmed trigger conditions becomes valid. A TDC with 5 nsec resolution is started by

[1] K. Geske, H. Riege, R. van Staa, The Digital Electronics of the H1 Streamer Tube Detector, H1LSTEC 90-8, 1990

the logical OR of all trigger conditions and stopped by the active edge of the HERA clock. The resulting 6 bit code is stored in the TDC Pipeline, the depth of which is one stage smaller than that of the Pattern Pipeline, because the TDC itself acts as the first pipeline stage.
For reasons of compatibility with the FPS electronics, the Pattern Pipeline has a width of 4 bytes, where in this application one byte is dummy. So the address space of the Trigger Board consists of 6 bytes, one for the Board Address, four for the Pattern Pipeline and one for the TDC Pipeline.

4) Crate Controller

Main parts of the Crate Controller are six registers, which store the necessary configuration parameters and a finite state machine *Manager*, which controls the pipeline register read-out.



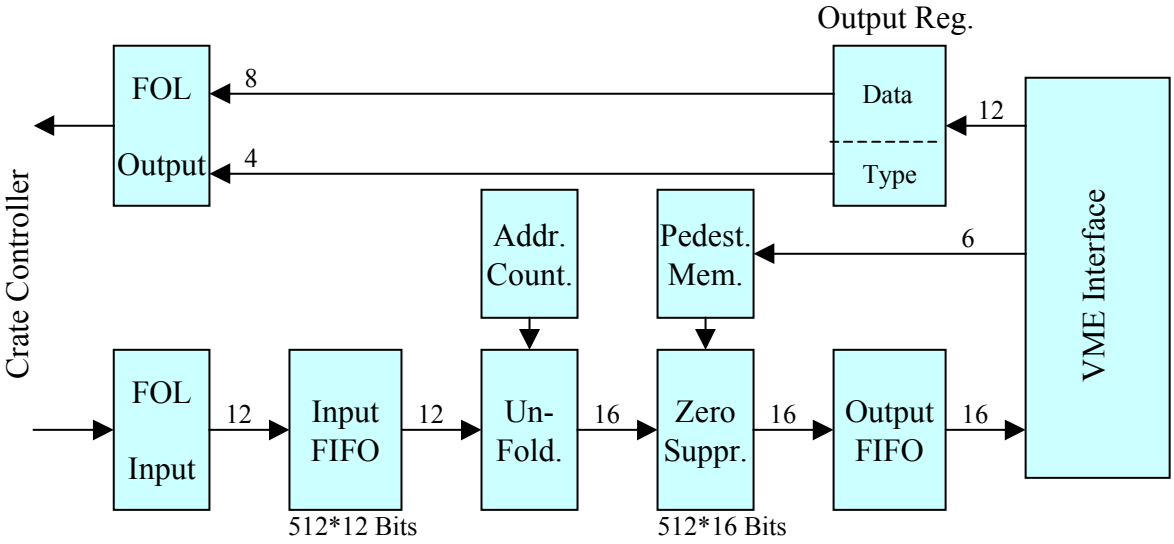
H1 Very Forward Proton Spectrometer VFPS
Crate Controller

The configuration registers are programmed via the Master Controller and the optical link. For verification purposes they can be read back on the same path.
The most important register is the Command Register, where the mode of operation can be selected. The Strobe Nr. Register defines the number of steps necessary to shift the data of the triggered event to the pipeline output register. By means of the Test Bit Register the Test Level input of individual channels on each Pipeline Board and the Hit Pattern on the Trigger Board can be activated. The Mask Register provides the 8 bit mask for different trigger decisions on the Trigger Board. The comparator thresholds, generated by two DAC´s, are issued via the Trigger Board to the Comparator Boards at the detector.
The finite state machine is clocked by the HERA clock and steered by ENPL (Enable Pipeline), a signal generated by the H1 Central Trigger Controller. If ENPL is true, *Manager* enables the event data to be shifted through the pipelines with HERA clock frequency. If a trigger occurs, ENPL goes false, and the pipelines are halted.
The data of the triggered event are now stored at a certain stage of the pipeline. In order to be able to read them out, *Manager* at first has to shift them to the pipeline end by issuing an appropriate number of strobe pulses STR, which is stored in Strobe Nr. Register. Then the Address Counter is set up, and the pipeline output registers are ad

dressed one after the other. For reasons of compatibility with FPS, 17 Pipeline Boards are read-out, even if not all are plugged in. The addresses of the missing boards are provided by a small additional Adapter. The data coming from the Pipeline Boards and the Trigger Board are transferred directly to the Master Controller via optical fiber.

5) Master Controller

The Master Controller provides the communication with the Front End Crate. It transmits configuration data and receives event data from the Crate Controller.



H1 Very Forward Proton Spectrometer VFPS

Master Controller

It mainly consists of an Output Register and two FIFO's with data reduction facility in between.. Value and Type of a data byte, which is to be sent to the front end registers, have to be written into the Output Register. The logic on the board then sequentially sends the data type and data value via a TAXI chip and a fiber optic link to the Crate Controller, where the data type is decoded as data destination and the value is stored in the corresponding register.

Data types and values, arriving sequentially at the input port of the board, are stored in parallel in the Input FIFO of 512 words length.

Optionally a zero suppression stage can be activated for data reduction. For that purpose a Pedestal Memory has been implemented, which provides for each PSPM channel the actual pedestal value. Only pixel data larger than the corresponding pedestal value are passed. In that mode the pixel values are unfolded from the 8 bit data frame and stored together with the pixel address in the Output FIFO.

The sequential data transfer rate is 100 MBaud.

6) Read-out Time

For calculation of the read-out time two contributions have to be considered:

- Transfer of data to the pipeline output (Strobe frequency is 5 MHz):
  At most 10 steps * 0.2 μsec = 2.0 μsec
- Data read-out (Frequency is 5 MHz):
  Pipeline Boards: 17 * 13 * 0.2 μsec = 44.2 μsec
  Trigger Board: 6 * 0.2 μsec = 1.2 μsec

This results in a maximum read-out time of 48 μsec per Pot. Since the read-out is done in parallel for both pots, it is also the maximum read-out time per event.

III. Data Acquisition

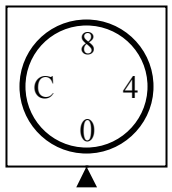
In the following chapter more detailed informations are given, which are necessary to program the system for data acquisition.

1) Programming the Master Controller

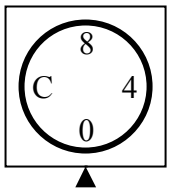
a) VME Programming

The Master Controller is a common VME Board of 6 height units. The VME interface supports Short Supervisory Access and Short Non Privileged Access (Address Modifiers $2D and $29 respectively). Interrupt handling is fully supported. Interrupt Level and Vector can be defined per software.

The Address Lines are fully decoded. The 8 most significant address bits can be selected by means of two hexadecimal switches on the board (see board layout scheme in the appendix):



SWH (A12..A15)



SWL (A8..A11)

The Base Address of the board can be calculated from the switch settings by the following formula:

Base Address = SWH*$1000 + SWL*$100

The complete Instruction Address is then given by

Instruction Address = Base Address + Addr,

where **Addr** is listed in the following table:

Instruction	Ad	A7	A6	A5	A4	A3	A2	A1	Acc
General Clear	0	0	0	0	0	0	0	0	write
Write Command Register	2	0	0	0	0	0	0	1	write
Read Command Register	2	0	0	0	0	0	0	1	read
Read Status Register	6	0	0	0	0	0	1	1	read
Write Output Register	8	0	0	0	0	1	0	0	write
Clear FIFO's	A	0	0	0	0	1	0	1	write
Read Output FIFO	A	0	0	0	0	1	0	1	read
Clear Interrupt Flag	C	0	0	0	0	1	1	0	write
Write Pedestal Memory	E	0	0	0	0	1	1	1	write
Read Pedestal Memory	E	0	0	0	0	1	1	1	read
Set Local Mode	14	0	0	0	1	0	1	0	write
Read Word Count Register	16	0	0	0	1	0	1	1	read

Table 1: Instruction Table

The instructions are shortly described in the following:

General Clear (Addr. 0)
Resets all registers, counters and flags on the board, but not the FIFO's.

Read/Write Command Register (Addr. 2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEN	**IL2**	**IL1**	**IL0**	**NDAT**	**TRON**	**IER3**	**ADF**	**IV7**	**IV6**	**IV5**	**IV4**	**IV3**	**IV2**	**IV1**	**IV0**

IV7..IV0: Interrupt Vector
ADF: All Data Flag 0: Zero Suppression
1: No Zero Suppression
IER3: Inhibit Error 3 0: Check Addresses of Pipeline Boards
1: Inhibit the Board Address Check
TRON: Trigger Data Only 0: Expect FADC Data after Trigger Data
1: Expect only Trigger Data.
Attention: TRON=1 makes only sense, if the **RTO** flag on the Crate Controller is also set (See description there). Otherwise data confusion will occur. **RTO** has to be set after **TRON**.
NDAT: No Data Flag 0: FADC Data passed
1: FADC Data suppressed.
IL2..IL0: Interrupt Level
IEN: Interrupt Enabled 0: Interrupt disabled
1: Interrupt enabled
The only interrupt source is the **DFNE** flag (see Status Register)

Read Status Register (Addr. 6)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NIFF	**NIFE**	**x**	**ERR5**	**ERR4**	**ERR3**	**ERR2**	**ERR1**	**NOFF**	**NOFE**	**0**	**DFNE**	**DT3**	**DT2**	**DT1**	**DT0**

DT3..DT0: Data Type of last received data byte (see Table 2)
DFNE: Delta FIFO not Empty 0: Output FIFO is empty
1: Output FIFO became empty
This transition flag is the interrupt source
It is cleared by the command 'Clear Interrupt Flag'
NOFE: Not Output FIFO Empty 0: Output FIFO is empty
1: Output FIFO is not empty
NOFF: Not Output FIFO Full 0: Output FIFO is full
1: Output FIFO is not full
ERR1: Error Flag 1 1: Wrong Data Type
ERR2: Error Flag 2 1: Wrong Trigger Board Address
ERR3: Error Flag 3 1: Wrong Pipeline Board Address
ERR4: Error Flag 4 not implemented
ERR5: Error Flag 5 1: Pedestal Memory Address has reached its maximum value
The Error Flags are reset by the Command 'General Clear'.
NIFE: Not Input FIFO Empty 0: Input FIFO is empty
1: Input FIFO is not empty
NIFF: Not Input FIFO Full 0: Input FIFO is full
1: Input FIFO is not full

Write Output Register (Addr. 8)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	**x**	**x**	**x**	**DT3**	**DT2**	**DT1**	**DT0**	**DV7**	**DV6**	**DV5**	**DV4**	**DV3**	**DV2**	**DV1**	**DV0**

DV7..DV0: Data Value to be transferred to the Crate Controller
DT3..DT0: Data Type which is encoded by the Crate Controller. (see Table 2)
DT3 determines the direction of transfer:
DT3=0: Write Access to the Registers on the Crate Controller (Type 2..7)
DT3=1: Type 10..15: Initiates a read access to the Control Registers, the read result is stored in the Output FIFO.(DV7..DV0 meaningless).

Data Type	DT3..DT0	Description
2	0010	Write Crate Controller Command Register
3	0011	Write DAC 0 Register
4	0100	Write DAC 1 Register (not used in VFPS)
5	0101	Write Trigger Mask Register
6	0110	Write Shift Number Register
7	0111	Write Test Bit Register
8	1000	Event Data
A	1010	Read Crate Controller Command Register
B	1011	Read DAC 0 Register
C	1100	Read DAC 1 Register (not used in VFPS)
D	1101	Read Trigger Mask Register
E	1110	Read Shift Number Register
F	1111	Read Test Bit Register

Table 2: Legal Data Types

Clear FIFO's (Addr. $A)

This dataless command clears the Input FIFO and the Output FIFO. Additionally it resets the **DFNE** flag, the Word Count Register and the Pedestal Memory Address Counter. During normal read-out operation this function is not used, but only in case of an error.

Clear Interrupt Flag (Addr. $C)

This dataless resets the **DFNE** flag and the Word Count Register.

Read/Write Pedestal Memory (Addr. $E)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**PED5**	**PED4**	**PED3**	**PED2**	**PED1**	**PED0**

PED7.. PED0: Pedestal Values
In Zero Suppression Mode data are transferred to the Output FIFO, only if its value is larger than the corresponding pedestal.
The correlation between memory address **MA** and FADC Nr. **NA** (0 <= NA <= 15) on Pipeline Board with address **PAD** (1<= PAD <= 17) is given by the formula:

MA = (**PAD**-1)*16 + **NA**

So at most 272 bytes of the 1kB memory are used. The memory address counter is incremented by each read or write access. So before any read or write cycle the counter has to be reset by the command 'Clear FIFO's'.

Set Local Mode (Addr. $14)

This dataless command sets an internal flag to inhibit the common L2 Reject input, which is used to stop the event data read-out in case of trigger abort. It could be used for local testing purposes, if one wants to have the full data read-out despite of trigger abort.
The flag is reset by the command 'General Clear'.

Read Word Count Register (Addr. $16)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**WC8**	**WC7**	**WC6**	**WC5**	**WC4**	**WC3**	**WC2**	**WC1**	**WC0**

WC8.. WC0: 9 Bit Word count
During event processing in Zero Suppression Mode, the number of words transferred to the Output FIFO is counted by a Word Counter. At the end of the procedure the counting result, reduced by 2, is written into the Word Count Register and can be read out via VME. So the content of the register is zero as long as data reduction is going on. The register is cleared automatically, when a new event read-out starts.
In case of an error found during data reduction the register contains only the number of words transferred before the error occurred. All subsequent data, which are transferred without zero suppression, are not counted.

Read Output FIFO (Addr. $A)

The data of one event (one time slice in the Event Pipeline) have a fixed structure, which is different for Normal Mode and Error Mode. The format of data stored in the Output FIFO is described in the following.
At first, in both operation modes, the following 6 Trigger Board data are found:

Trigger Board Address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**

Hit Pattern

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**T2d**	**T2c**	**T2b**	**T2a**	**T1d**	**T1c**	**T1b**	**T1a**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**T4d**	**T4c**	**T4b**	**T4a**	**T3d**	**T3c**	**T3b**	**T3a**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**

T1a.. T1d: Trigger Tiles, 1. layer, u-coordinate
T2a.. T2d: Trigger Tiles, 1. layer, v-coordinate
T3a.. T3d: Trigger Tiles, 2. layer, u-coordinate
T4a.. T4d: Trigger Tiles, 2. layer, v-coordinate

Trigger Pattern

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**TP7**	**TP6**	**TP5**	**TP4**	**TP3**	**TP2**	**TP1**	**TP0**

TP7.. TP0: Trigger Conditions 0: Trigger condition was false
1: Trigger condition was true

TDC Value

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**TDAV**	**TDC4**	**TDC3**	**TDC2**	**TDC1**	**TDC0**

TDC4.. TDC0: TDC Measurement
TDAV: Data Valid 0: Measurement is not valid
1: Measurement is valid

The format of the following FADC data depends on the operation mode. In Normal Mode the number of entries is not predictable and can be read-out from the Word Count Register. Each word contains the address and value of a pixel:

FADC Entry in Normal Mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD9	**AD8**	**AD7**	**AD6**	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

D5.. D0: FADC Value
AD9..AD0: Pixel Address
The correlation between pixel address **PA** and FADC Nr. **NA** (1 <= NA <= 16) on Pipeline Board with address **PAD** (1<= PAD <= 17) is given by the formula:

PA = (**PAD**-1)*16 + **NA.**

The last word in Normal Mode is always the End of Transfer Word (EOT Word):

EOT Word in Normal Mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**ERR5**	**ERR4**	**ERR3**	**ERR2**	**ERR1**

ERR5.. ERR1: Error Code 0: No Error
1: Error detected (see Status Register)

If no Error Bit is set the transfer came to a legal end.
If during data transfer an error is encountered, the Master Controller switches to Error Mode, sends the EOT Word, which flags the error type, and transmits the remaining data from the Input FIFO to the Output FIFO without any modification in order to provide the raw data for error analysis.
In Error Mode the data are stored in the Output FIFO as they are sent by the Crate Controller and received by the Input FIFO. For each Pipeline Board at first the Board Address is transferred:

Pipeline Board Address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**PAD4**	**PAD3**	**PAD2**	**PAD1**	**PAD0**

PAD4.. PAD0: 5 bit Board Address (1 <= PAD <= 17)

Since the values of 4 FADC are packed into 3 bytes, the pixel data are sent in block of 3 bytes:

Pipeline Board Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**AD11**	**AD10**	**AD05**	**AD04**	**AD03**	**AD02**	**AD01**	**AD00**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**AD23**	**AD22**	**AD21**	**AD20**	**AD15**	**AD14**	**AD13**	**AD12**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**AD35**	**AD34**	**AD33**	**AD32**	**AD31**	**AD30**	**AD25**	**AD24**

AD05.. AD00: FADC Value of 1. Pixel
AD15.. AD10: FADC Value of 2. Pixel
AD25.. AD20: FADC Value of 3. Pixel
AD35.. AD30: FADC Value of 4. Pixel

So for each Pipeline Board four such blocks are transmitted.

In Error Mode the transfer is not finished by an EOT Word, but the data have to be read until the Output FIFO is empty (**NOFE** flag in Status Register).

b) Recommendations and Hints

- In order to obtain pedestal values, one should at first run without Zero Suppression **(ADF**=1) .
- There are two possibilities to get only trigger data:
  Set **RTO** flag on the Crate Controller and **TRON** flag on the Master Controller. Then only trigger data are sent from the Crate Controller to the Master Controller and the transfer time is shorter, but the **RTO** flag has to be set again before each transfer (it is automatically reset after each transfer).
  Set the **NDAT** flag on the Master Controller. Then the complete data set is transmitted from the Crate Controller to the Master Controller, but only trigger data are passed to the Output FIFO (in both operation modes). The transfer time is longer, but the flag has to be set only once.
- In Normal Mode the correct appearance of the Pipeline Board addresses is checked. In case of an error, this operation mode is aborted and Error Mode is activated. If there is a permanently faulty Pipeline Board, one can suppress the check by setting the **IERR3** flag in order to be able to run further in Normal Mode. But one has to take into account, that data integrity now is reduced.

2) Operating the Crate Controller

The Crate Controller in the main module in the Front End Crate and serves the following purposes:

- Storage of configuration data sent by the Master Controller.
- Retransmission of configuration parameters on request of the Master Controller.
- Start of test cycles forced by the Master Controller.
- In case of a trigger read-out and transmission of trigger and FADC data.

a) Registers

There are several Configuration Registers, which are programmed by writing the configuration parameter together with the corresponding Data Type (2..7) to the Output Register of the Master Controller. Retransmission is initiated by writing the corresponding Data Type (10..15) to the Output Register (see Table 2).

Write Command Register (Type 2)

7	6	5	4	3	2	1	0
SCLR	**0**	**0**	**RTO**	**LED**	**TST**	**ROT**	**DAQ**

DAQ: Data Acquisition
0: disabled
1: enabled. Data Acquisition is steered by the H1 control signal ENPL (Enable Pipeline):
ENPL goes true: Data are shifted through the Pipeline
ENPL goes false: Data read-out is started

ROT: Read one more time
0: disabled
1: Data of the next time slice are read out.
The procedure is started only, if **ENPL**=0.
ROT is reset automatically at the end of the read-out cycle.

TST: Test Mode
0: disabled
1: For test purposes the following artificial events are read-out:
Pedestal Event: **LED**=0, Test Bits reset

Test Event: **LED**=0, Test Bits set
LED Event: **LED**=1, Test Bits reset
The procedure is started only, if **ENPL**=0 and **DAQ**=0.
TST is reset automatically at the end of the read-out cycle.

LED: LED Pulse Mode — 0: LED Pulse Generator switched off
1: LED Pulse Generator switched on

RTO: Read Trigger Data only — 0: disabled
1: Only trigger data (the first six words of event data) are transmitted in **DAQ**, **ROT** or **TST** cycle.
RTO is reset automatically at the end of the read-out cycle.

SCLR: Soft Clear — By setting **SCLR**=1 and **SCLR**=0 in a sequence the state machines and the Command Register on the board are reset. It is recommended to issue a soft clear sequence after power-on.
Attention: Leaving **SCLR**=1 disables the board completely!

Read Command Register (Type 10)

7	6	5	4	3	2	1	0
ST2	**ST1**	**ENPL**	**RTO**	**LED**	**TST**	**ROT**	**DAQ**

The first five bits are displaying the current status of the command bits. Additional Status Bits are:

ENPL: Enable Pipeline — 0: Pipeline is disabled
1: Pipeline is enabled

ST2,ST1: Status Bits for diagnostic purposes

DAC Registers

The Crate Controller is equipped with two 8 bit DAC's, which provide two thresholds for the comparators of the trigger detector signals. With a sensitivity of 10 mV/LSB, the maximum output voltage is 2.55 V. The DAC voltage is issued via the Trigger Board to the Comparator Boards, which are mounted in the detector box and attenuate the voltage by a factor of 10, giving a maximum comparator threshold of 255 mV. DAC0 (Type 3) provides a negative threshold for the trigger tile detectors, while the positive voltage of DAC1 (Type 4) is not used by VFPS.
The DAC's can be programmed by writing the appropriate data byte to the DAC Registers. Their content can be verified by reading them back (Type 11 and 12 respectively).

7	6	5	4	3	2	1	0
DAC7	**DAC6**	**DAC5**	**DAC4**	**DAC3**	**DAC2**	**DAC1**	**DAC0**

DAC7..DAC0: DAC Bits — 0: 0 mV Output
255: 255 mV Output

Trigger Mask Register

The Trigger Mask Register serves the purpose to individually enable each of the 8 different trigger conditions by setting the corresponding Mask Bit (Type 5). The content of the register can be verified by reading it back (Type 13).

7	6	5	4	3	2	1	0
M7	**M6**	**M5**	**M4**	**M3**	**M2**	**M1**	**M0**

M7..M0: Mask Bits — 0: Corresponding trigger condition disabled
1: Corresponding trigger condition enabled

Shift Number Register

The Shift Number Register has to be programmed by writing the number of steps necessary to shift the data of the triggered event to the Pipeline end (Type 6). Only the six least significant bits are used. The register can be read back for verification (Type 14).

7	6	5	4	3	2	1	0
0	**0**	**SN5**	**SN4**	**SN3**	**SN2**	**SN1**	**SN0**

SN5..SN0: Shift Number

Test Bit Register

The Test Bit Register has been implemented to provide well known conditions for test events. Both write access (Type 7) and read access (Type 15) are supported.

7	6	5	4	3	2	1	0
TB7	**TB6**	**TB5**	**TB4**	**TB3**	**TB2**	**TB1**	**TB0**

TB7..TB00: Test Bits 0: Test Bit deactivated
1: Test Bit activated

On the Trigger Board a Test Bit emulates two trigger detector hits. On the Pipeline Boards it applies a test voltage of about 0.5 V to the FADC input of two channels. The correlation between Test Bits and Pipeline Board channels or Trigger Board inputs is given in the following table:

TB	Pipeline Board Channel	Trigger Board Channel
0	0,8	T1a,T1c
1	1,9	T1b,T1d
2	2,10	T2a,T2c
3	3,11	T2b,T2d
4	4,12	T3a,T3c
5	5,13	T3b,T3d
6	6,14	T4a,T4c
7	0,15	T4b,T4d

Table 3: Correlation between Trigger Bits and Board Inputs

b) Jumpers

There are two groups of jumper locations on the board (see board layout in the appendix). In each group exactly one jumper has to be set.

Clock Jumper

Selects the source oh the main clock signal:

HCLK (J1): H1 Clock, received via fiber optic link from the STC Crate
OCLK (J2): Artificial oscillator clock on board
ECLK (J3): External clock supplied at front connector

LED Clock Delay

The delay of the LED output pulse can be selected in steps of 5 nsec in order to be able to adjust the LED detector signal to the FADC clock.
J13: 5 nsec, J12: 10 nsec, ...J4: 50 nsec.

c) Front Panel

LED Status Display
There are three red LED's showing (from bottom to top) the state of the Status Bits **ENPL**, **ST1** and **ST2**.

ECLK Connector (P4)
TTL Input. This (upper) connector can be used as system clock input, if jumper **J3** is set.

ENPL~ Connector (P3)
TTL Output. This connector has been implemented for inspection of the (active low) **ENPL** (Enable Pipeline) level.

LEDP Connector (P5)
NIM Output. Has to be connected to the LED Pulse Generator by a LEMO cable.

TAXI Connector
Bi-directional port for the optical fiber connection with the Master Controller.

3) Operating the Trigger Board

a) Trigger Processor

The Trigger Board provides the trigger decision for one Roman Pot. As inputs for the Trigger Processor the digital signals of the following trigger tile detectors are used:

T1a.. T1d: 1. layer, u-coordinate
T2a.. T2d: 1. layer, v-coordinate
T3a.. T3d: 2. layer, u-coordinate
T4a.. T4d: 2. layer, v-coordinate

There are 8 different trigger conditions **TP7..TP0,** which are described as logical equations of the input variables and implemented as firmware in the Trigger Processor CPLD. They are activated, if **TST**=0 in the Crate Controller Command Register.
For **TST**=1 the trigger condition are simply defined by the following equation:

$$\mathbf{TPn} = \mathbf{TBn} \quad (n = 0..7)$$

where **TBn** are the Test Bits.

b) Front Panel

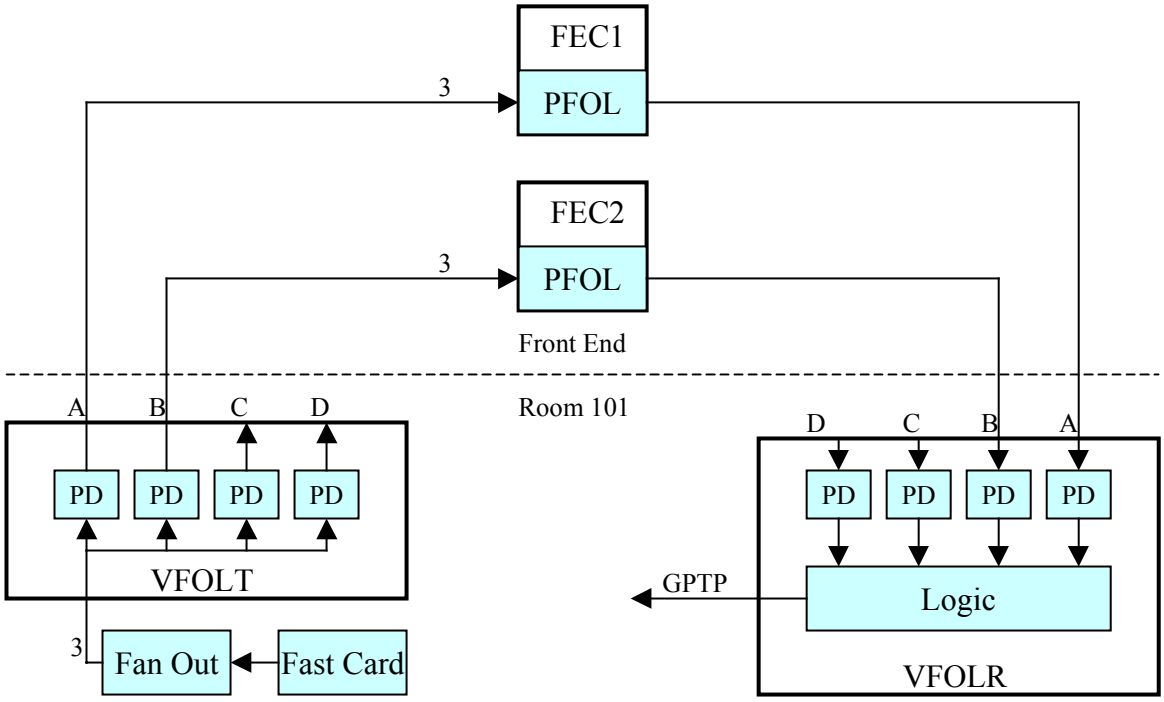
Threshold Inspects
Analog Outputs. Two LEMO Connectors for monitoring the output voltage of the threshold DAC's.

Detector Inputs
Two 40-fold flat cable connectors (P3, P4). On these connectors the digital trigger detector signals coming from the Comparator Boards are received. In the other direction the two threshold voltages are supplied to the comparators.

Monitor Connector
One 34-fold flat cable connectors (P5). It provides the trigger detector signals as outputs and has to be connected to the Trigger Rate Monitor in the Control Room.

4) The Fiber Optic Control System

The Fiber Optic Control System distributes via optical fibers the control signals **HCLK** (H1 system clock), **ENPL** (Enable Pipeline) and **FCLR** (Fast Clear) to the Front End Crates and receives the trigger signals from the Trigger Boards. It can operate up to four Pots in parallel. For VFPS only two channels are used:



H1 Very Forward Proton Spectrometer VFPS

Fiber Optic Control System

The three signals **HCLK**, **ENPL** and **FCLR** coming from the STC Fast Card, are led through the STC Fan Out Board to the VME Board **VFOLT** (VME Fiber Optic Link Transmitter), which provides four identical channels, each equipped with three programmable Delay Lines **PD**. The control signals passing the delay circuits are converted to light pulses and transmitted via optical fibers to a front end receiver station **PFOL**, where they are reconverted and distributed in the Front End Crate **FEC**. The correct delay value has to be find out by varying the delay, until the mean FADC output gets an optimum.

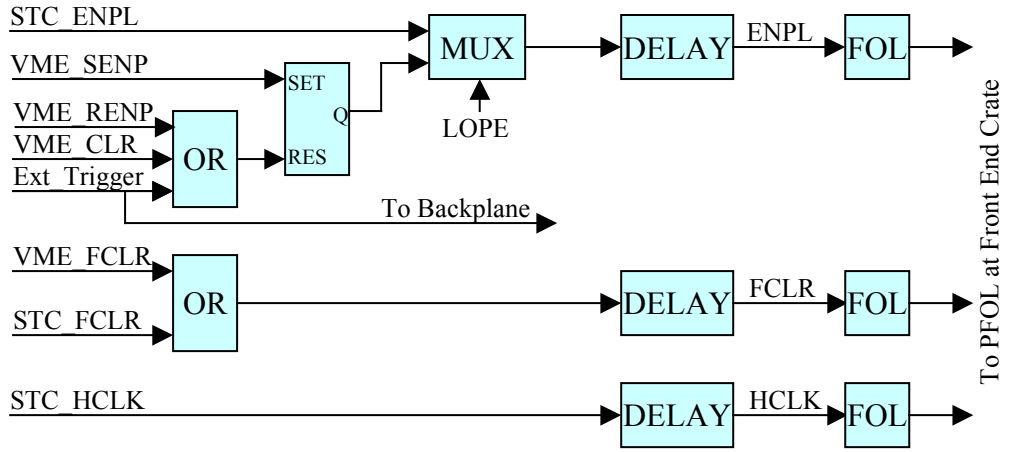
On the other hand, trigger signals generated by the Trigger Board of the Front End Crates are sent via optical fiber to the VME module **VFOLR** (VME Fiber Optic Link Receiver), located again in the STC crate in Room 101. **VFOLR** also provides for each channel one programmable delay **PD**, which enables one to compensate for the different arrival times of the trigger pulses. The delay values can be programmed in steps of 5 nsec in order to get an optimum overlap of the trigger pulses, which can be observed by means of four monitor outputs at the module.

The four trigger signals, which can be masked by software, are connected to a logic unit, where by firmware 8 different logical combinations are implemented, the result of

which are provided as 8 separate TTL signals at the backplane connector P2 for transferring to the General Purpose Trigger Pipeline **GPTP**. For test purposes the logical OR of all unmasked input signal can be monitored at the front panel.

4.1) VFOLT

The VME Fiber Optic Link Transmitter is a VME Board of 6 height units, which resides in the STC Crate in the Control Room 101. It issues the three necessary control signals to the Front End Crates, as shown in the following block diagram for one of four channels:



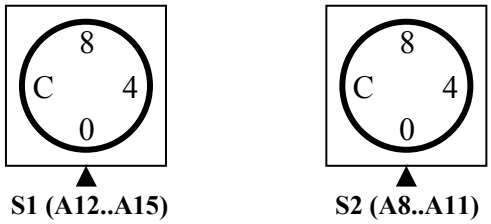
H1 Very Forward Proton Spectrometer VFPS

VFOLT (1 of 4 channels)

The actual **ENPL** level can be generated either in Normal Mode (**LOPE**=0) by the corresponding STC signal **STC_ENPL**, coming from the STC Fast Card, or in Local Mode (**LOPE**=1) by a FLIP FLOP, which is set by a VME command (**VME_SENP**) and reset by an external trigger signal, the VME command **VME_RENP** or the VME Clear instruction **VME_CLR**. The control signal **FCLR** is the logical OR of the STC signal **STC_FCLR** and the VME command **VME_FCLR**. Finally the system clock **HCLK** is driven by the H1 clock **STC_HCLK**, also coming from the STC Fast Card.
The trigger signal **EXT_Trigger** is provided by the **VFOLR** module (see next section). Via Backplane it is connected to the STC Fast Card.

a) VME Programming

The VME interface supports Short Supervisory Access and Short Non Privileged Access (Address Modifiers $2D and $29 respectively
The Address Lines are fully decoded. The 8 most significant address bits can be selected by means of two hexadecimal switches on the board (see board layout scheme in the appendix):



The default value is $30;

The Base Address of the board can be calculated from the switch settings by the following formula:

Base Address = S1*$1000 + S2*$100

The complete Instruction Address is then given by

Instruction Address = Base Address + Addr,

where **Addr** is listed in the following table:

Instruction	Ad	A7	A6	A5	A4	A3	A2	A1	Acc
Write Delay A for **FCLR**	0	0	0	0	0	0	0	0	write
Read Delay A for **FCLR**	0	0	0	0	0	0	0	0	read
Write Delay B for **FCLR**	2	0	0	0	0	0	0	1	write
Read Delay B for **FCLR**	2	0	0	0	0	0	0	1	read
Write Delay C for **FCLR**	4	0	0	0	0	0	1	0	write
Read Delay C for **FCLR**	4	0	0	0	0	0	1	0	read
Write Delay D for **FCLR**	6	0	0	0	0	0	1	1	write
Read Delay D for **FCLR**	6	0	0	0	0	0	1	1	read
Write Delay A for **ENPL**	8	0	0	0	0	1	0	0	write
Read Delay A for **ENPL**	8	0	0	0	0	1	0	0	read
Write Delay B for **ENPL**	A	0	0	0	0	1	0	1	write
Read Delay B for **ENPL**	A	0	0	0	0	1	0	1	read
Write Delay C for **ENPL**	C	0	0	0	0	1	1	0	write
Read Delay C for **ENPL**	C	0	0	0	0	1	1	0	read
Write Delay D for **ENPL**	E	0	0	0	0	1	1	1	write
Read Delay D for **ENPL**	E	0	0	0	0	1	1	1	read
Write Delay A for **HCLK**	10	0	0	0	1	0	0	0	write
Read Delay A for **HCLK**	10	0	0	0	1	0	0	0	read
Write Delay B for **HCLK**	12	0	0	0	1	0	0	1	write
Read Delay B for **HCLK**	12	0	0	0	1	0	0	1	read
Write Delay C for **HCLK**	14	0	0	0	1	0	1	0	write
Read Delay C for **HCLK**	14	0	0	0	1	0	1	0	read
Write Delay D for **HCLK**	16	0	0	0	1	0	1	1	write
Read Delay D for **HCLK**	16	0	0	0	1	0	1	1	read
Write Command Register	18	0	0	0	1	1	0	0	write
Read Command Register	18	0	0	0	1	1	0	0	read
Clear	1A	0	0	0	1	1	0	1	write
Read Status Register	1A	0	0	0	1	1	0	1	read
Set Local Pipeline Enable **ENPL**	1C	0	0	0	1	1	1	0	write
Reset Local Pipeline Enable **ENPL**	1E	0	0	0	1	1	1	1	write
Generate **FCLR**	20	0	0	1	0	0	0	0	write

Table 4: Instruction Table of VFOLT

The instructions are shortly described in the following:

Read/Write Delay Registers (Addr. 0 ... Addr. $16)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**D4**	**D3**	**D2**	**D1**	**D0**

D4..D0: Delay Value **DV** ($0 \le DV \le 19$)
The signal delay can be programmed is steps of 5 nsec. The resulting delay is given by the formula Delay = DV * 5 nsec.
Numbers lager than 19 are forced to 19.

Read/Write Command Registers (Addr. $18)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOPE	**x**	**x**	**x**	**E3D**	**E3C**	**E3B**	**E3A**	**E2D**	**E2C**	**E2B**	**E2A**	**E1D**	**E1C**	**E1B**	**E1A**

E1A..E1D: Output Enable 0: The fiber optic link output **FCLR** of channels A..D is disabled.
1: The fiber optic link output **FCLR** of channels A..D is enabled.
E2A..E2D: Output Enable 0: The fiber optic link output **ENPL** of channels A..D is disabled.
1: The fiber optic link output **ENPL** of channels A..D is enabled.
E3A..E3D: Output Enable 0: The fiber optic link output **HCLK** of channels A..D is disabled.
1: The fiber optic link output **HCLK** of channels A..D is enabled.
LOPE: Local Mode 0: Local Mode disabled. **ENPL** is forced by the STC Fast Card.
1: Local Mode enabled. **ENPL** is forced by the local **ENPL** Flip Flop.

Read Status Registers (Addr. $1A)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**ENPL**	**LPEN**

LPEN: Local **ENPL** 0: Local **ENPL** FLIP-FLOP is reset.
1: Local **ENPL** FLIP-FLOP is set..
ENPL: Enable Pipeline 0: The **ENPL** level, transmitted to the Front End is 0.
1: The **ENPL** level, transmitted to the Front End is 1.

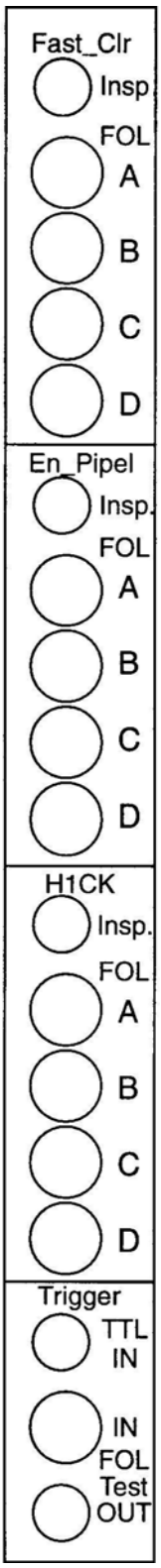
Clear (Addr. $1A)
This instruction performs a general clear on the board. Especially a state machine, the Command Register and the Delay Registers are reset. The instruction should be issued once at program start.

Set Local Pipeline Enable (Addr. $1C)
The local **ENPL** FLIP-FLOP is set. It forces the transmitted **ENPL** level only, if the Local Mode (**LOPE** in the Command Register) has been set.

Reset Local Pipeline Enable (Addr. $1E)
The local **ENPL** FLIP-FLOP is reset. It forces the transmitted **ENPL** level only, if the Local Mode (**LOPE** in the Command Register) has been set.

Generate FCLR (Addr. $20)
A **FCLR** signal is transmitted to the Front End in both operation modes (independent of **LOPE** in the Command Register).

b) Front Panel



Insp:	Undelayed **FCLR**	0,5 V @ 50 Ω	LEMO Output
A..D:	Delayed **FCLR**	FOL	FOL Output
Insp:	Undelayed **ENPL**	0,5 V @ 50 Ω	LEMO Output
A..D:	Delayed **ENPL**	FOL	FOL Output
Insp:	Undelayed **HCLK**	0,5 V @ 50 Ω	LEMO Output
A..D:	Delayed **HCLK**	FOL	FOL Output

Trigger:	**VFOLR** Trigger	TTL	LEMO Input
Test In:	**VFOLT** Signal	Light	FOL Input
Test Out:	**VFOLT** Signal	TTL	LEMO Output

c) Jumper

There are a few jumpers on the board, which have to be configured.

Clock Selection

One and only one of the following three jumpers has to be closed:

J10: **HCLK** is generated by internal 10 MHz oscillator (STC Fast Card is missing)
J11: **HCLK** is generated by inverted H1 Clock, coming from STC Fast Card
J12: **HCLK** is generated by non inverted H1 Clock, coming from STC Fast Card

Inverter

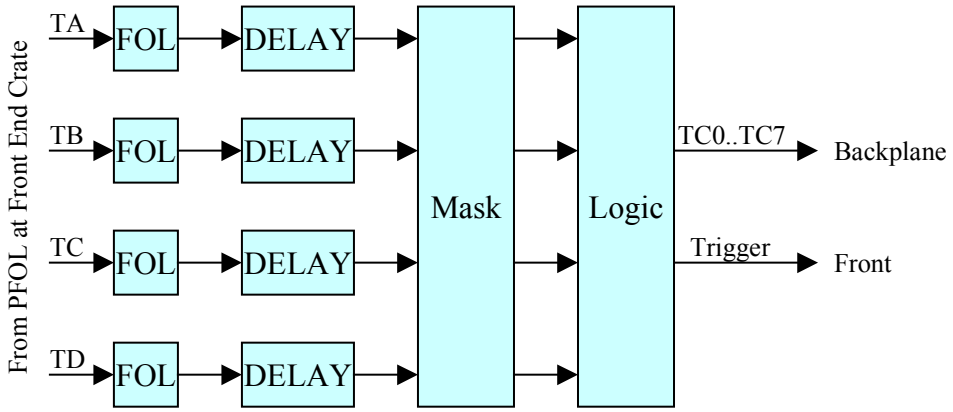
J21:	open:	Delayed Output **FCLR** is not inverted
	Closed:	Delayed Output **FCLR** is inverted
J22:	open:	Delayed Output **ENPL** is not inverted
	Closed:	Delayed Output **ENPL** is inverted
J23:	open:	Delayed Output **HCLK** is not inverted
	Closed:	Delayed Output **HCLK** is inverted

Internal Configuration

J23..J35: always closed

4.2) VFOLR

The Fiber Optic Link Receiver **VFOLR** can receive up to 4 trigger signals coming from the **PFOL** modules of Front End Crates. After passing programmable delays for optimum time adjustment and a programmable mask for individual input selection, they are connected to a logic unit, where up to 8 different logical combinations are defined by firmware. The resulting trigger pattern **TC0..TC7** is provided at the STC Crate Backplane for transmission to the H1 General Purpose Trigger Processor **GPTP**.

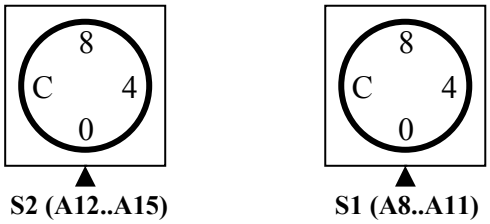


H1 Very Forward Proton Spectrometer VFPS
VFOLR

Th logical OR of the trigger combinations is the final trigger signal, which is output at the front panel and has to be connected to the **VFOLT** module by a LEMO cable.

a) VME Programming

The VME interface supports Short Supervisory Access and Short Non Privileged Access (Address Modifiers $2D and $29 respectively



The Address Lines are fully decoded. The 8 most significant address bits can be selected by means of two hexadecimal switches on the board (see board layout scheme in the appendix):

The Base Address of the board can be calculated from the switch settings by the following formula:

Base Address = S2*$1000 + S1*$100

The complete Instruction Address is then given by

Instruction Address = Base Address + Addr,

where **Addr** is listed in the following table:

Instruction	Ad	A7	A6	A5	A4	A3	A2	A1	Acc
Write Delay A	0	0	0	0	0	0	0	0	write
Read Delay A	0	0	0	0	0	0	0	0	read
Write Delay B	4	0	0	0	0	0	1	0	write
Read Delay B	4	0	0	0	0	0	1	0	read
Write Delay C	8	0	0	0	0	1	0	0	write
Read Delay C	8	0	0	0	0	1	0	0	read
Write Delay D	C	0	0	0	0	1	1	0	write
Read Delay D	C	0	0	0	0	1	1	0	read
Write Mask Register	10	0	0	0	1	0	0	0	write
Read Mask Register	10	0	0	0	1	0	0	0	read
Clear	1A	0	0	0	1	1	0	1	write

Table 5: Instruction Table of VFOLR

The instructions are shortly described in the following:

Read/Write Delay Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**D4**	**D3**	**D2**	**D1**	**D0**

D4..D0: Delay Value **DV** ($0 \le DV \le 19$)
The signal delay can be programmed is steps of 5 nsec. The resulting delay is given by the formula Delay = DV * 5 nsec.
Numbers lager than 19 are forced to 19.

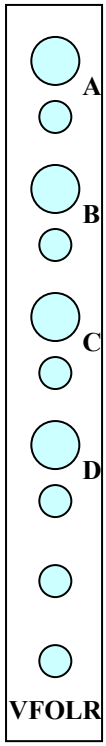
Read/Write Mask Register (Addr. $10)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**x**	**END**	**ENC**	**ENB**	**ENA**

ENA..END: Enable 0: Trigger input signal on channel A..D is disabled.
1: Trigger input signal on channel A..D is enabled.

Clear (Addr. $1A)
This instruction performs a general clear on the board. Especially a state machine, the Command Register and the Delay Registers are reset. The instruction should be issued once at program start.

b) Front Panel



Trigger A:	FOL Input	FOL Connector
Delayed Trigger A:	NIM Output	LEMO
Trigger B:	FOL Input	FOL Connector
Delayed Trigger B:	NIM Output	LEMO
Trigger C:	FOL Input	FOL Connector
Delayed Trigger C:	NIM Output	LEMO
Trigger D:	FOL Input	FOL Connector
Delayed Trigger D:	NIM Output	LEMO
Trigger:	NIM Output	LEMO
Trigger:	TTL Output	LEMO

c) Backplane Outputs

The following table shows the logical functions of the masked inputs **TA..TD** together with the corresponding pin numbers, provided at the backplane connector P2.

Function	Pin	Function	Pin
TA	P2 c8	GND	P2 a8
TB	P2 c7	GND	P2 a7
TC	P2 c6	GND	P2 a6
TD	P2 c5	GND	P2 a5
TC & TD	P2 c4	GND	P2 a4
TA & TB	P2 c3	GND	P2 a3
TA & TC & TD	P2 c2	GND	P2 a2
TA & TB & TC & TD	P2 c1	GND	P2 a1

Table 6: Logical Combinations of TA..TD

d) Jumpers

There are ten jumpers on the boards for internal configuration (see layout in the appendix). They have to be set in the following manner:

J3:	closed
J1, J4:	open
J2, J5:	open
J8:	closed
J7, J10:	open
J6, J9:	open

IV. First Steps

The following first steps are suggested for system configuration and verification.

1) Register Test

Program all Crate Controller registers and verify the content by reading them back.

2) Pedestal Events

Set Test Bit Register = 0
Shift Nr. Register = 42
ADF=1 in **MC** Command Register
TST=1 in **CC** Command Register

One should observe, that

- The **NOFE** flag in the Status Register of the Master Controller becomes true
- A data set is stored in the Output FIFO
- The CC Command Register has been cleared

For the event data set one can expect, that

- The first Trigger Word **T1** shows the Board Address $14
- The next five Trigger Words **T2..T6** are 0
- The Pixel Data are showing pedestal values, with exception of those representing Board Addresses.

3) Test Events

Set Test Bit Register = **TB**>0
Shift Nr. Register = 1
ADF=1 in **MC** Command Register
DAQ=1 in **CC** Command Register
LOPE=1 in **VFOLT** Command Register
Local **ENPL** on **VFOLT** Board
Reset Local **ENPL** on **VFOLT** Board

Expected results:

- **T1**: $14
- **T2,T3**: according to Table 3
- **T4**: 0
- **T5**: **TB**
- **T6:** a value between 1 and 19
- **Pixel:** about 36 for those channels, which have been stimulated (see Table 3)

4) LED Events

Set Test Bit Register = 0
Shift Nr. Register = 1
ADF=1 in **MC** Command Register
DAQ=1 in **CC** Command Register
LED=1 in **CC** Command Register
LOPE=1 in **VFOLT** Command Register
Local **ENPL** on **VFOLT** Board

Reset Local **ENPL** on **VFOLT** Board

Expected results:

- **T1**: $14
- **T2..T6**: 0
- **Pixel**: Pedestal values with exception of those, which are illuminated by LED's Since the time interval between two LED pulses is 4*96 nsec, one should get LED events only in every fourth time slice.

5) Physics Events

Before getting really physics data, one has do the following two tasks:

- Determination of the Pipeline stage, where data of triggered events are stored
- Adjustment of the FADC conversion strobe to the analog pixel signal maximum.

a) Determination of Shift Number

Set Test Bit Register = 0
Shift Nr. Register = 1
DAQ=1 in **CC** Command Register
RTO=1 in **CC** Command Register

After a trigger only the trigger data of the last Pipeline stage are written to the Output FIFO of the Master Controller. Then the trigger data of all other Pipeline stages can be read out by consecutively starting new read-out cycles by setting

ROT=1 in **CC** Command Register
RTO=1 in **CC** Command Register.

Plotting for many events the number of observed trigger pattern versus the stage number, one should get a clear peak at a certain Shift Number **SN**, which then has to be written to the Shift Nr. Register for physics data acquisition.

b) Determination of H1 clock delay

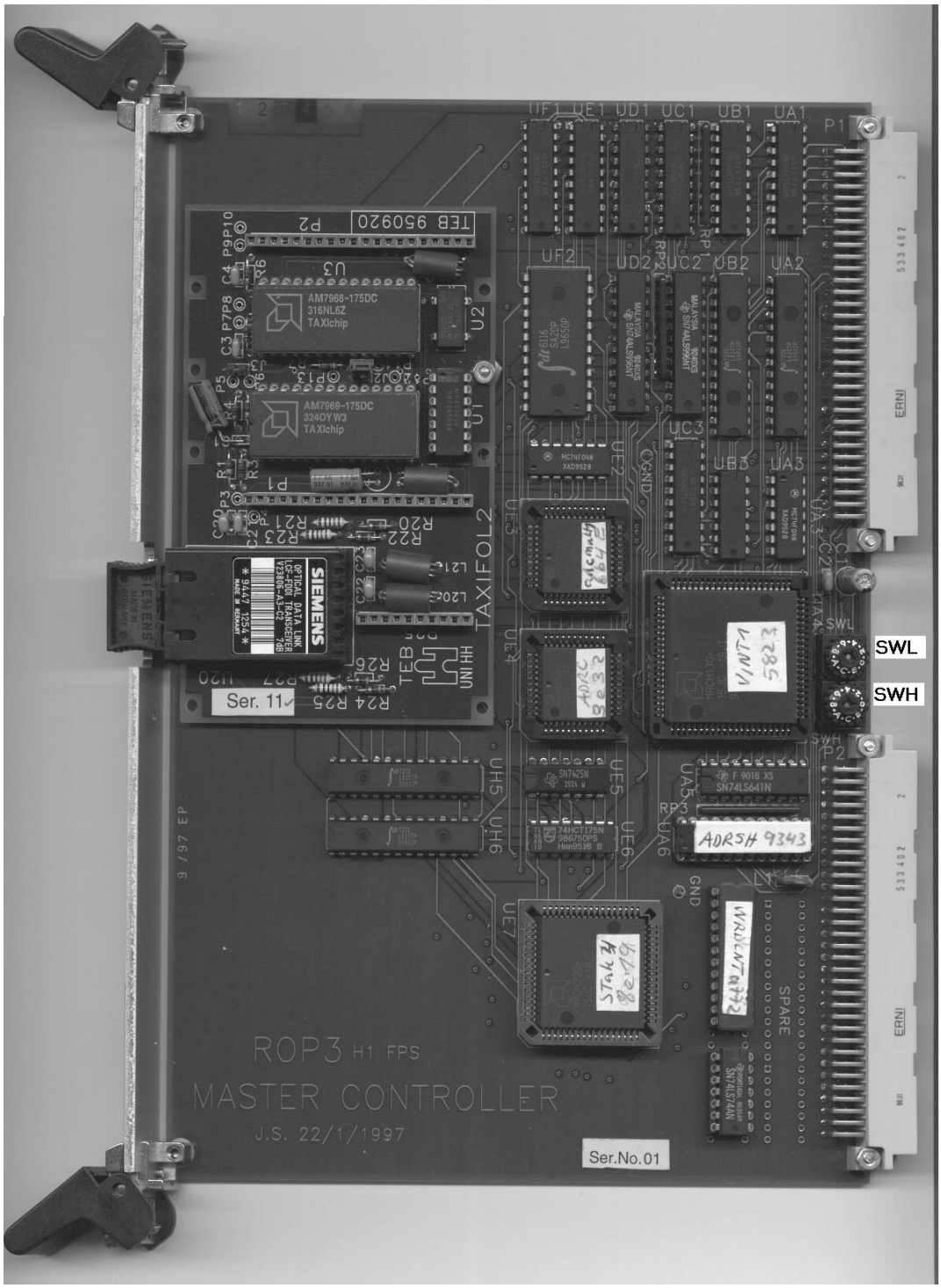
Since the FADC conversion strobe is derived from the H1 system clock, the time adjustment of the FADC clock to the pixel signals is done by programming the delay of the control signals **HCLK**, **ENPL** and **FCLR** on the **VFOLT** board.

Set Test Bit Register = 0
Shift Nr. Register = **SN**
DAQ=1 in **CC** Command Register

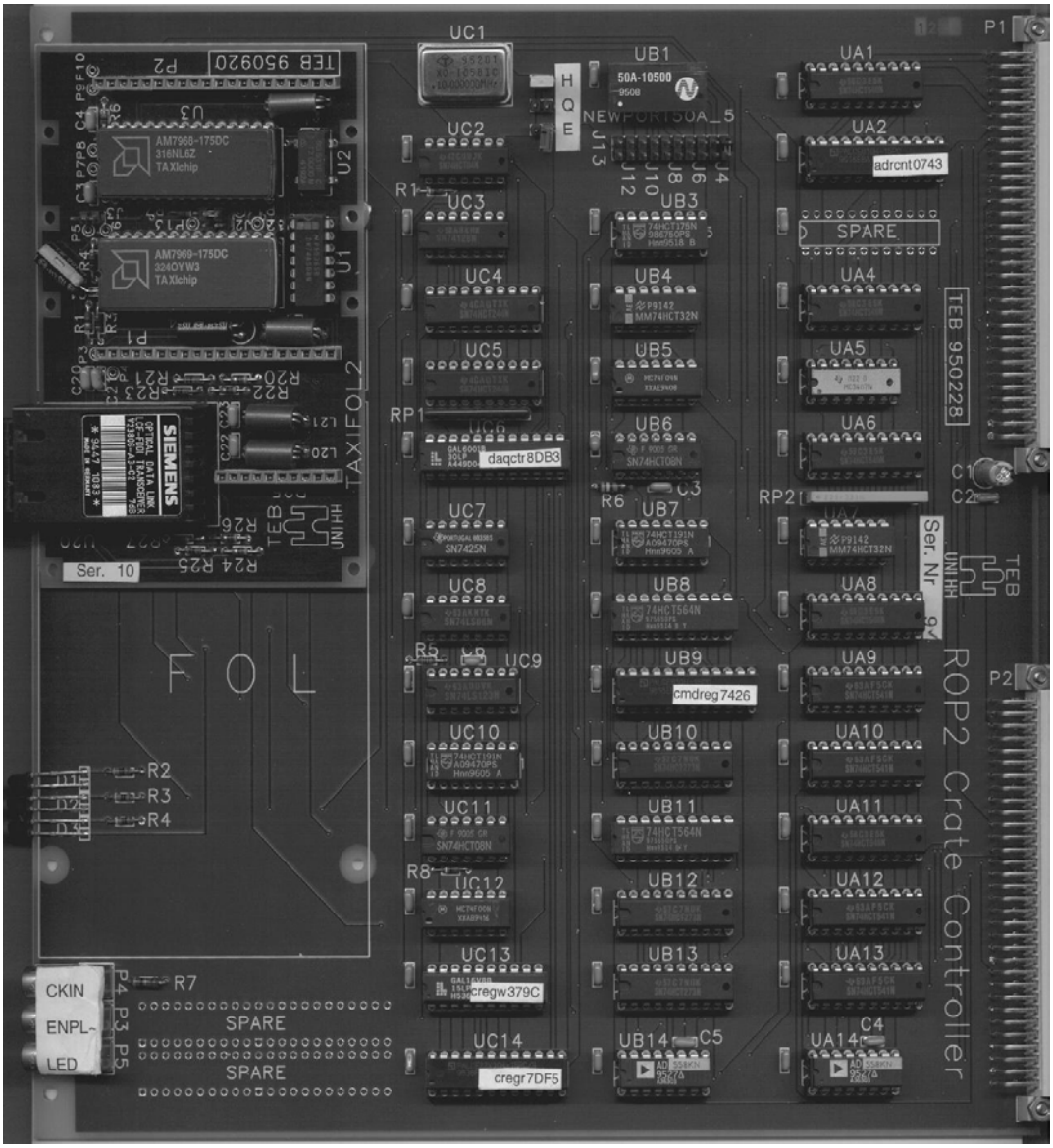
After a trigger the complete data set of the correct Pipeline stage is written to the Output FIFO of the Master Controller. One has to plot for many events the mean pixel amplitude versus the **HCLK** delay and should get a broader maximum around the optimum delay value, which then should be used for physics data acquisition.
In principle that procedure has to be done for each Pot individually.

V. Appendix

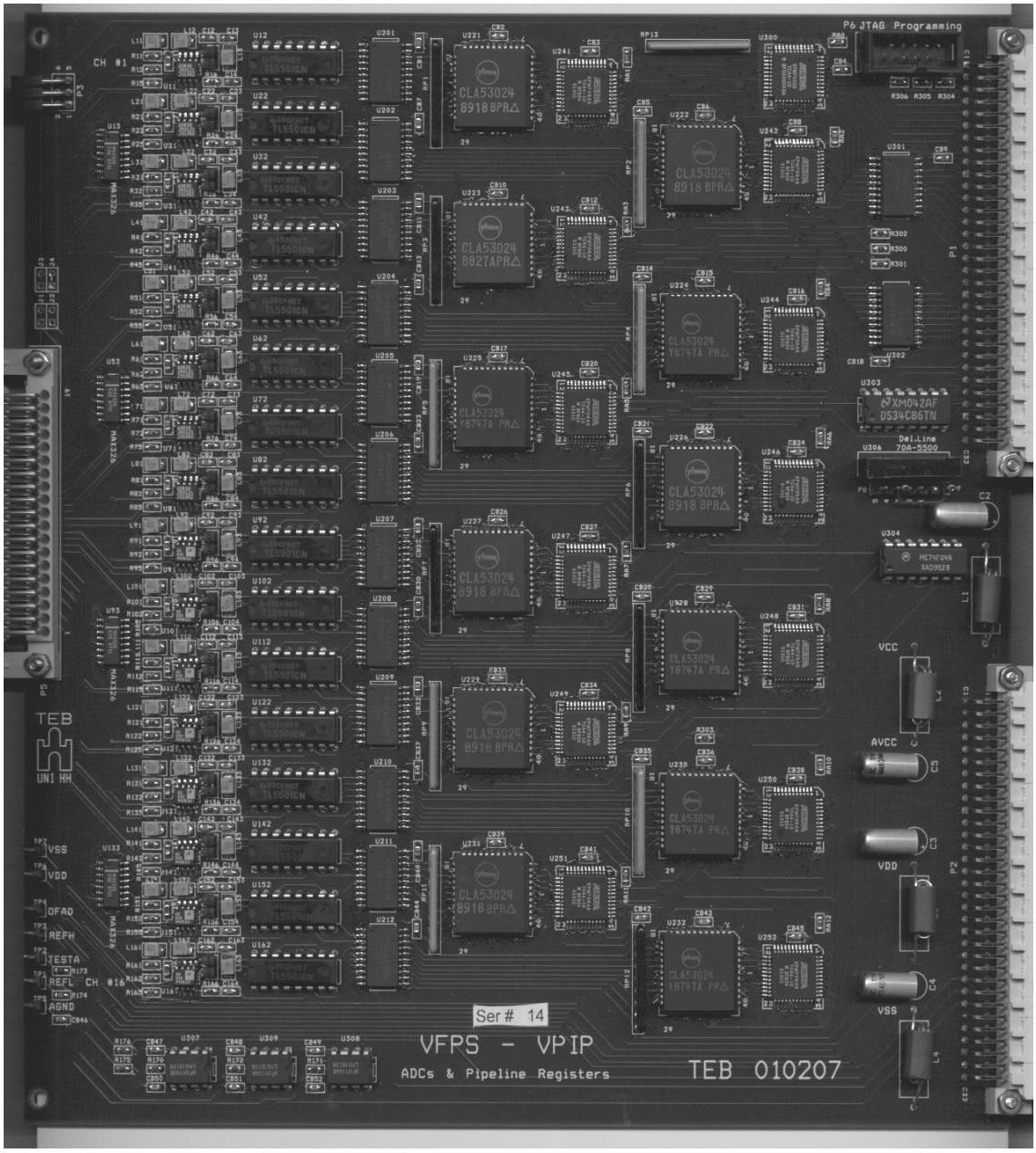
1) Master Controller Board Layout



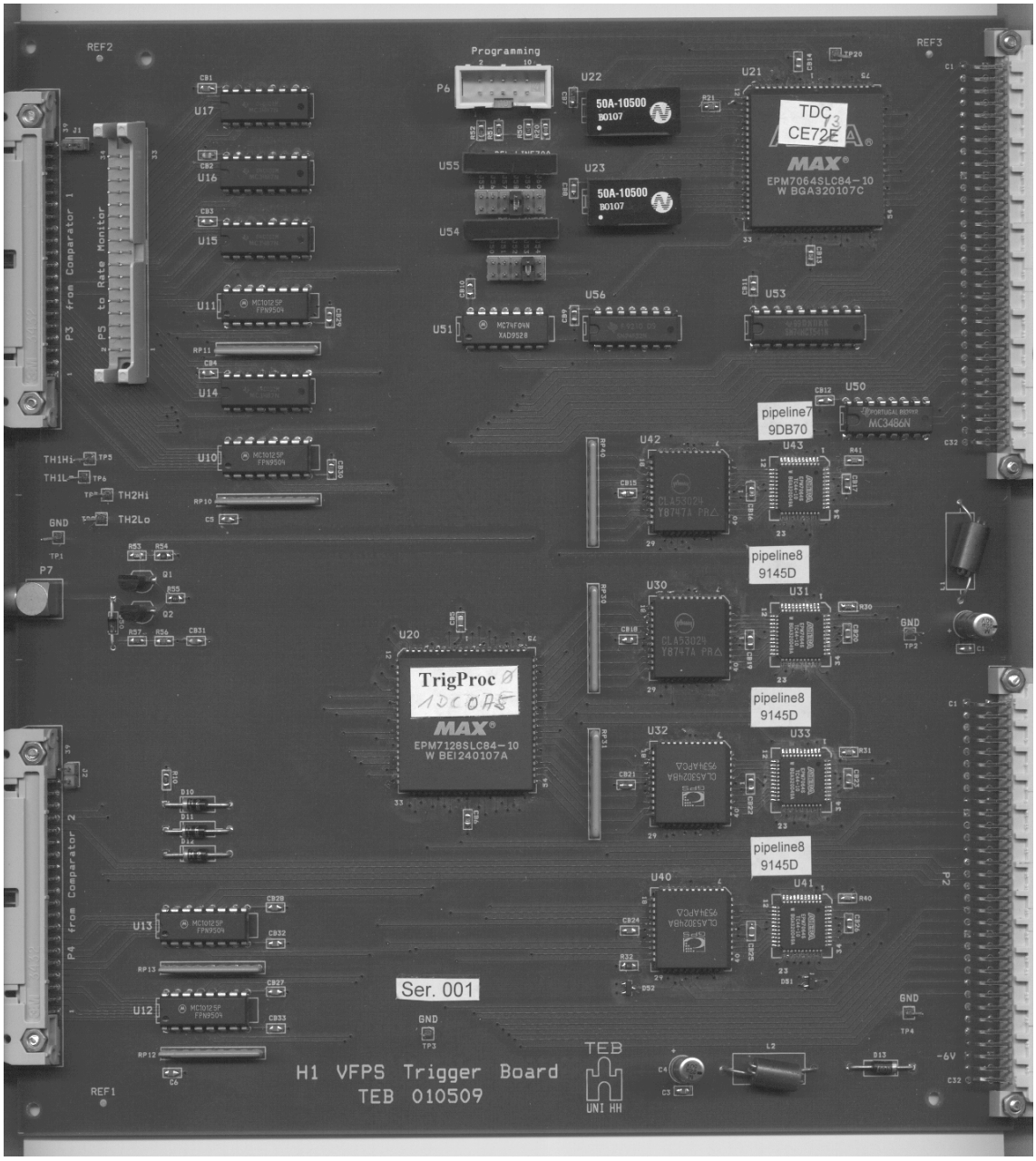
2) Crate Controller Board Layout



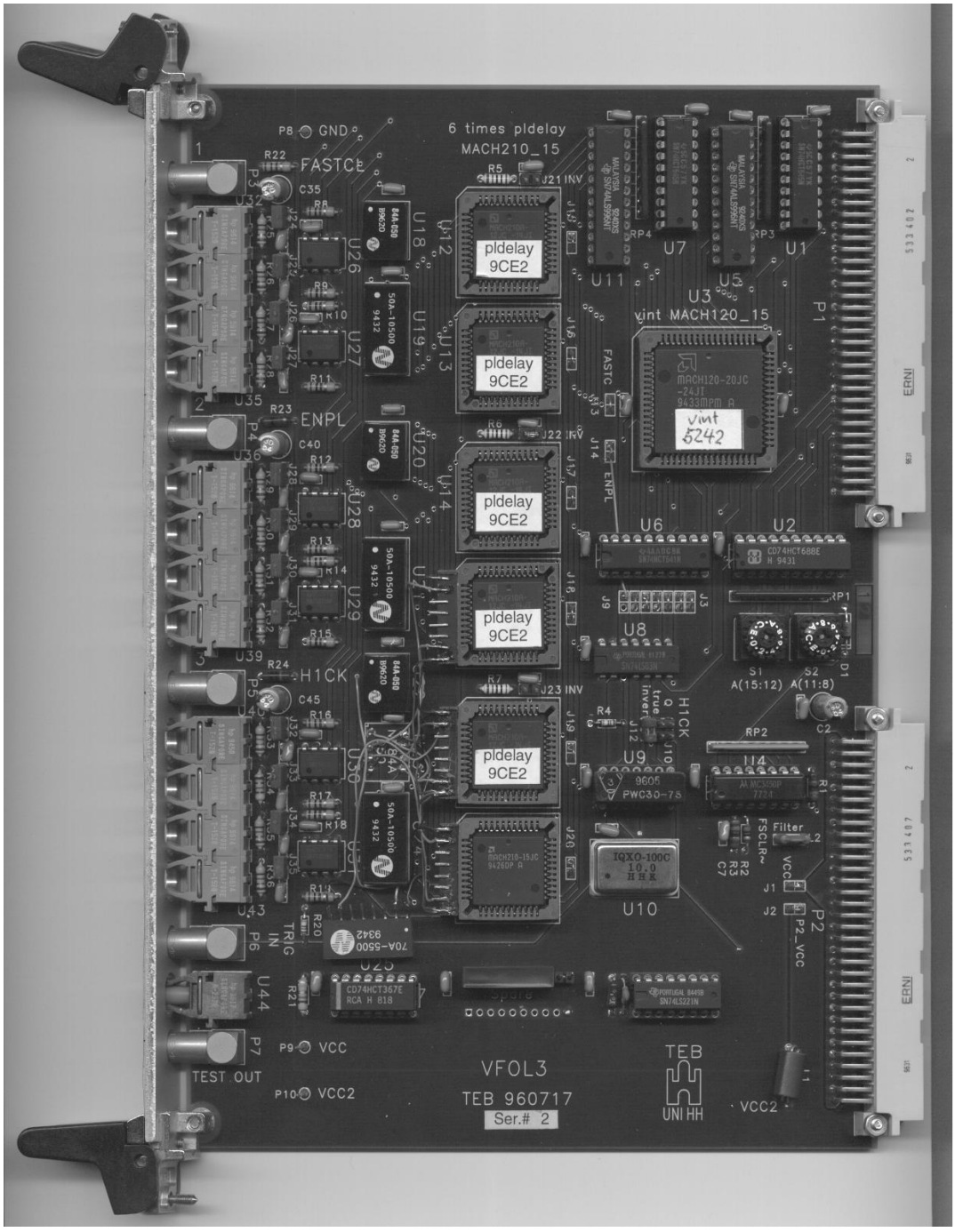
3) Pipeline Board Layout



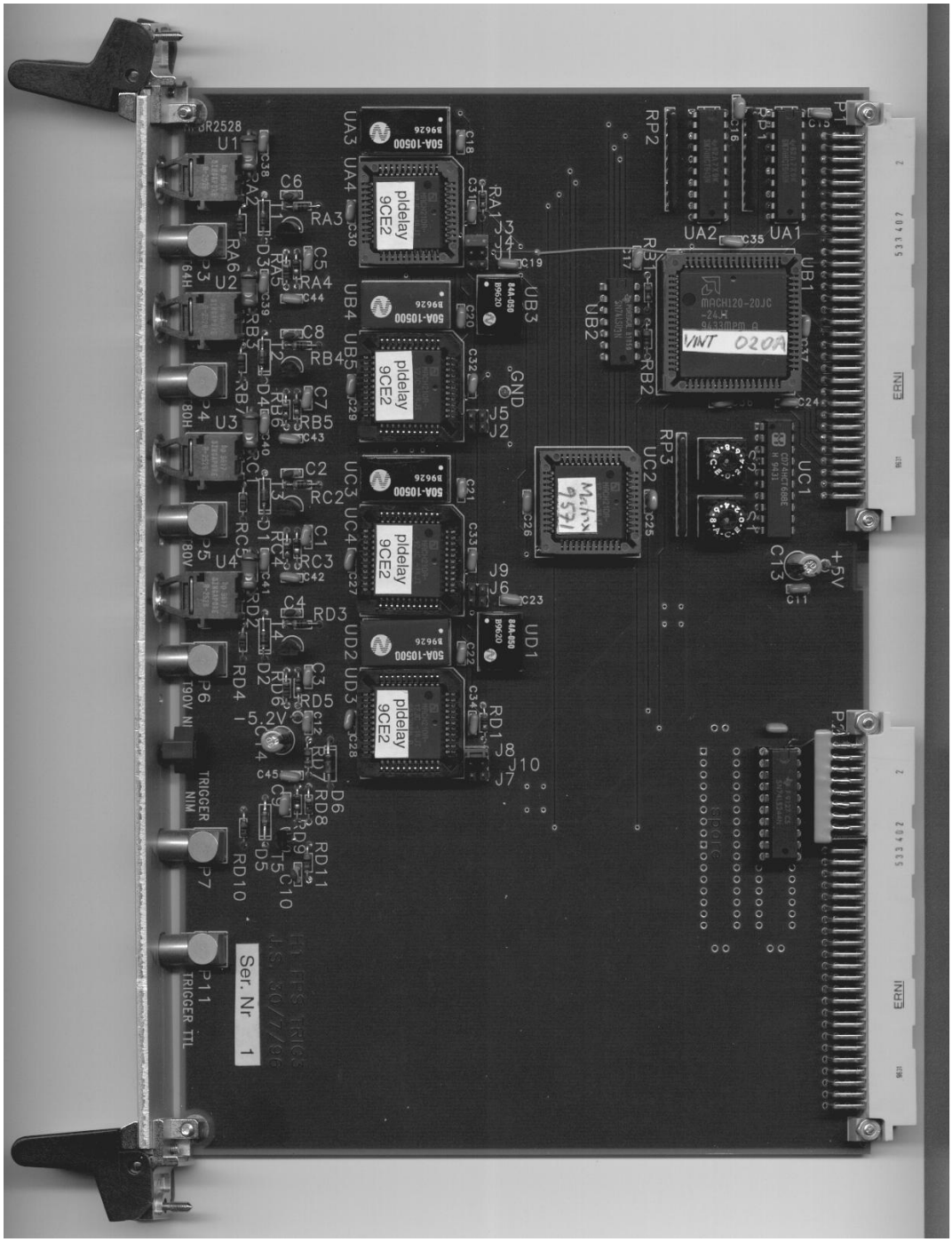
4) Trigger Board Layout



5) VFOLT Board Layout



6) VFOLR Board Layout



7) PSPM Allocation

Detector A (220 m)

PSPM Name	PSPM Label	Adapter	Preamp Input	Flange	Pipeline Board
P1	KA2384	B	b17-b32	P1	1
P2	KA2352	A	b1-b16	P2	2
P3	KA2192	A	b1-b16	P3	3
P4	KA2365	B	b17-b32	P4	4
P5	KA2332	A	b1-b16	P5	5
P6	KA2185	B	b17-b32	P6	6
P7	KA2183	B	b17-b32	P7	7
P8	KA2411	A	b1-b16	P8	8

Detector B (224 m)

PSPM Name	PSPM Label	Adapter	Preamp Input	Flange	Pipeline Board
P1	KA2198	B	b17-b32	P1	1
P2	KA2293	A	b1-b16	P2	2
P3	KA2317	A	b1-b16	P3	3
P4	KA2229	B	b17-b32	P4	4
P5	KA2464	A	b1-b16	P5	5
P6	KA2482	B	b17-b32	P6	6
P7	KA2193	B	b17-b32	P7	7
P8	KA2475	A	b1-b16	P8	8

8) Signal Table

PSPM 1

Fibers				PSPM		Ampl. Inp.		Flange		Pipeline Board		FADC
				Nr.	Pixel	Con.	Pin	Con.	Pin +,-	Card	Pin +,-	Channel
1	31	61	91	1	1	P1	b17	P1	16,35	1	16,35	1
9	39	69	99		2		b18		15,34		15,34	2
3	33	63	93		3		b19		14,33		14,33	3
11	41	71	101		4		b20		13,32		13,32	4
5	35	65	95	1	5	P1	b21	P1	12,31	1	12,31	5
13	43	73	101		6		b22		11,30		11,30	6
7	37	67	97		7		b23		10,29		10,29	7
15	45	75	105		8		b24		9,28		9,28	8
2	32	62	92	1	9	P1	b25	P1	8,27	1	8,27	9
10	40	70	100		10		b26		7,26		7,26	10
4	34	64	94		11		b27		6,25		6,25	11
12	42	72	102		12		b28		5,24		5,24	12
6	36	66	96	1	13	P1	b29	P1	4,23	1	4,23	13
14	44	74	104		14		b30		3,22		3,22	14
8	38	68	98		15		b31		2,21		2,21	15
LED L1					16		b32		1,20		1,20	16

PSPM 2

Fibers				PSPM		Ampl. Inp.		Flange		Pipeline Board		FADC
				Nr.	Pixel	Con.	Pin	Con.	Pin +,-	Card	Pin +,-	Channel
16	46	76	106	2	1	P1	b01	P2	16,35	2	16,35	1
24	54	84	114		2		b02		15,34		15,34	2
18	48	78	108		3		b03		14,33		14,33	3
26	56	86	116		4		b04		13,32		13,32	4
20	50	80	110	2	5	P1	b05	P2	12,31	2	12,31	5
28	58	88	118		6		b06		11,30		11,30	6
22	52	82	112		7		b07		10,29		10,29	7
30	60	90	120		8		b08		9,28		9,28	8
17	47	77	107	2	9	P1	b09	P2	8,27	2	8,27	9
25	55	85	115		10		b10		7,26		7,26	10
19	49	79	109		11		b11		6,25		6,25	11
27	57	87	117		12		b12		5,24		5,24	12
21	51	81	111	2	13	P1	b13	P2	4,23	2	4,23	13
29	59	89	119		14		b14		3,22		3,22	14
23	53	83	113		15		b15		2,21		2,21	15
LED L2					16		B16		1,20		1,20	16

PSPM 3

Fibers				PSPM		Ampl. Inp.		Flange		Pipeline Board		FADC
				Nr.	Pixel	Con.	Pin	Con.	Pin +,-	Card	Pin +,-	Channel
1	31	61	91	3	1	P1	b17	P3	16,35	3	16,35	1
9	39	69	99		2		b18		15,34		15,34	2
3	33	63	93		3		b19		14,33		14,33	3
11	41	71	101		4		b20		13,32		13,32	4
5	35	65	95	3	5	P1	b21	P3	12,31	3	12,31	5
13	43	73	101		6		b22		11,30		11,30	6
7	37	67	97		7		b23		10,29		10,29	7
15	45	75	105		8		b24		9,28		9,28	8
2	32	62	92	3	9	P1	b25	P3	8,27	3	8,27	9
10	40	70	100		10		b26		7,26		7,26	10
4	34	64	94		11		b27		6,25		6,25	11
12	42	72	102		12		b28		5,24		5,24	12
6	36	66	96	3	13	P1	b29	P3	4,23	3	4,23	13
14	44	74	104		14		b30		3,22		3,22	14
8	38	68	98		15		b31		2,21		2,21	15
LED L3					16		b32		1,20		1,20	16

PSPM 4

Fibers				PSPM		Ampl. Inp.		Flange		Pipeline Board		FADC
				Nr.	Pixel	Con.	Pin	Con.	Pin +,-	Card	Pin +,-	Channel
16	46	76	106	4	1	P1	b01	P4	16,35	4	16,35	1
24	54	84	114		2		b02		15,34		15,34	2
18	48	78	108		3		b03		14,33		14,33	3
26	56	86	116		4		b04		13,32		13,32	4
20	50	80	110	4	5	P1	b05	P4	12,31	4	12,31	5
28	58	88	118		6		b06		11,30		11,30	6
22	52	82	112		7		b07		10,29		10,29	7
30	60	90	120		8		b08		9,28		9,28	8
17	47	77	107	4	9	P1	b09	P4	8,27	4	8,27	9
25	55	85	115		10		b10		7,26		7,26	10
19	49	79	109		11		b11		6,25		6,25	11
27	57	87	117		12		b12		5,24		5,24	12
21	51	81	111	4	13	P1	b13	P4	4,23	4	4,23	13
29	59	89	119		14		b14		3,22		3,22	14
23	53	83	113		15		b15		2,21		2,21	15
LED L4					16		B16		1,20		1,20	16

PSPM 5

Fibers				PSPM		Ampl. Inp.		Flange		Pipeline Board		FADC
				Nr.	Pixel	Con.	Pin	Con.	Pin +,-	Card	Pin +,-	Channel
1	31	61	91	5	1	P1	b17	P5	16,35	5	16,35	1
9	39	69	99		2		b18		15,34		15,34	2
3	33	63	93		3		b19		14,33		14,33	3
11	41	71	101		4		b20		13,32		13,32	4
5	35	65	95	5	5	P1	b21	P5	12,31	5	12,31	5
13	43	73	101		6		b22		11,30		11,30	6
7	37	67	97		7		b23		10,29		10,29	7
15	45	75	105		8		b24		9,28		9,28	8
2	32	62	92	5	9	P1	b25	P5	8,27	5	8,27	9
10	40	70	100		10		b26		7,26		7,26	10
4	34	64	94		11		b27		6,25		6,25	11
12	42	72	102		12		b28		5,24		5,24	12
6	36	66	96	5	13	P1	b29	P5	4,23	5	4,23	13
14	44	74	104		14		b30		3,22		3,22	14
8	38	68	98		15		b31		2,21		2,21	15
LED L5					16		b32		1,20		1,20	16

PSPM 6

Fibers				PSPM		Ampl. Inp.		Flange		Pipeline Board		FADC
				Nr.	Pixel	Con.	Pin	Con.	Pin +,-	Card	Pin +,-	Channel
16	46	76	106	6	1	P1	b01	P6	16,35	6	16,35	1
24	54	84	114		2		b02		15,34		15,34	2
18	48	78	108		3		b03		14,33		14,33	3
26	56	86	116		4		b04		13,32		13,32	4
20	50	80	110	6	5	P1	b05	P6	12,31	6	12,31	5
28	58	88	118		6		b06		11,30		11,30	6
22	52	82	112		7		b07		10,29		10,29	7
30	60	90	120		8		b08		9,28		9,28	8
17	47	77	107	6	9	P1	b09	P6	8,27	6	8,27	9
25	55	85	115		10		b10		7,26		7,26	10
19	49	79	109		11		b11		6,25		6,25	11
27	57	87	117		12		b12		5,24		5,24	12
21	51	81	111	6	13	P1	b13	P6	4,23	6	4,23	13
29	59	89	119		14		b14		3,22		3,22	14
23	53	83	113		15		b15		2,21		2,21	15
LED L6					16		B16		1,20		1,20	16

PSPM 7

Fibers				PSPM		Ampl. Inp.		Flange		Pipeline Board		FADC
				Nr.	Pixel	Con.	Pin	Con.	Pin +,-	Card	Pin +,-	Channel
1	31	61	91	7	1	P1	b17	P7	16,35	7	16,35	1
9	39	69	99		2		b18		15,34		15,34	2
3	33	63	93		3		b19		14,33		14,33	3
11	41	71	101		4		b20		13,32		13,32	4
5	35	65	95	7	5	P1	b21	P7	12,31	7	12,31	5
13	43	73	101		6		b22		11,30		11,30	6
7	37	67	97		7		b23		10,29		10,29	7
15	45	75	105		8		b24		9,28		9,28	8
2	32	62	92	7	9	P1	b25	P7	8,27	7	8,27	9
10	40	70	100		10		b26		7,26		7,26	10
4	34	64	94		11		b27		6,25		6,25	11
12	42	72	102		12		b28		5,24		5,24	12
6	36	66	96	7	13	P1	b29	P7	4,23	7	4,23	13
14	44	74	104		14		b30		3,22		3,22	14
8	38	68	98		15		b31		2,21		2,21	15
LED L7					16		b32		1,20		1,20	16

PSPM 8

Fibers				PSPM		Ampl. Inp.		Flange		Pipeline Board		FADC
				Nr.	Pixel	Con.	Pin	Con.	Pin +,-	Card	Pin +,-	Channel
16	46	76	106	8	1	P1	b01	P8	16,35	8	16,35	1
24	54	84	114		2		b02		15,34		15,34	2
18	48	78	108		3		b03		14,33		14,33	3
26	56	86	116		4		b04		13,32		13,32	4
20	50	80	110	8	5	P1	b05	P8	12,31	8	12,31	5
28	58	88	118		6		b06		11,30		11,30	6
22	52	82	112		7		b07		10,29		10,29	7
30	60	90	120		8		b08		9,28		9,28	8
17	47	77	107	8	9	P1	b09	P8	8,27	8	8,27	9
25	55	85	115		10		b10		7,26		7,26	10
19	49	79	109		11		b11		6,25		6,25	11
27	57	87	117		12		b12		5,24		5,24	12
21	51	81	111	8	13	P1	b13	P8	4,23	8	4,23	13
29	59	89	119		14		b14		3,22		3,22	14
23	53	83	113		15		b15		2,21		2,21	15
LED L8					16		B16		1,20		1,20	16

Trigger PM's

PM	Ampl. Inp.		Ampl. Outp.		Flange		Pipeline Board			FADC
	Con.	Pin	Con.	Pin +,-	Con.	Pin +,-	Card	Con	Pin +,-	Channel
T1	P1	b17	P2	64,63	P9	16,35	17	P5	16,35	1
T2		b18		62,61		15,34			15,34	2
T3		b19		60,59		14,33			14,33	3
T4		B20		58,57		13,32			13,32	4
T5	P1	B21	P2	56,55	P9	12,31	17	P5	12,31	5
T6		B22		54,53		11,30			11,30	6
T7		B23		52,51		10,29			10,29	7
T8		B24		50,49		9,28			9,28	8
T9	P1	B25	P2	48,47	P9	8,27	17	P5	8,27	9
T10		B26		46,45		7,26			7,26	10
T11		B27		44,43		6,25			6,25	11
T12		B28		42,41		5,24			5,24	12
T14	P1	B29	P2	40,39	P9	4,23	17	P5	4,23	13
T14		B30		38,37		3,22			3,22	14
T15		B31		36,35		2,21			2,21	15
T16		B32		34,33		1,20			1,20	16

9) HV Distribution and Rate Monitor

PSPM's Pot 220m

PSPM	CAEN HV Ch.	Mnemonic	HV Panel	Pot Plug	HV Cable
1	1	220PSPM1	1b	HV1	1
2	2	220PSPM2	1c	HV1	1
3	3	220PSPM3	2b	HV2	2
4	4	220PSPM4	2c	HV2	2
5	5	220PSPM5	3b	HV3	3
6	6	220PSPM6	3c	HV3	3
7	7	220PSPM7	4b	HV4	4
8	8	220PSPM8	4c	HV4	4

PM's Pot 220 m

PM	Plane	HV Ch.	Mnemonic	HV Panel	Pot Plug	HV Cable	Comp	Tr.-Board	Rate Mon.
T1	u1	9	220PM1	1d	HV1	1	A1	T1a	1
T2	u1	10	220PM2	1e	HV1	1	A2	T1b	2
T3	u1	11	220PM3	1f	HV1	1	A3	T1c	3
T4	u1	12	220PM4	1h	HV1	1	A4	T1d	4
T5	v1	13	220PM5	2d	HV2	2	A5	T2a	5
T6	v1	14	220PM6	2e	HV2	2	A6	T2b	6
T7	v1	15	220PM7	2f	HV2	2	A7	T2c	7
T8	v1	16	220PM8	2f	HV2	2	A8	T2d	8
T9	u2	17	220PM9	3d	HV3	3	B1	T3a	9
T10	u2	18	220PM10	3e	HV3	3	B2	T3b	10
T11	u2	19	220PM11	3f	HV3	3	B3	T3c	11
T12	u2	20	220PM12	3h	HV3	3	B4	T3d	12
T13	u2	21	220PM13	4d	HV4	4	B5	T4a	12
T14	u2	22	220PM14	4e	HV4	4	B6	T4b	14
T15	u2	23	220PM15	4f	HV4	4	B7	T4c	15
T16	u2	24	220PM16	4h	HV4	4	B8	T4d	16

PSPM's Pot 224m

PSPM	CAEN HV Ch.	Mnemonic	HV Panel	Pot Plug	HV Cable
1	25	224PSPM1	5b	HV1	5
2	26	224PSPM2	5c	HV1	5
3	27	224PSPM3	6b	HV2	6
4	28	224PSPM4	6c	HV2	6
5	29	224PSPM5	7b	HV3	7
6	30	224PSPM6	7c	HV3	7
7	31	224PSPM7	8b	HV4	8
8	32	224PSPM8	8c	HV4	8

PM's Pot 224 m

PM	Detect.	HV Ch.	Mnemonic	HV Panel	Pot Plug	HV Cable	Comp	Tr.-Board	Rate Mon.
T1	u1	33	224PM1	5d	HV1	5	A1	T1a	1
T2	u1	34	224PM2	5e	HV1	5	A2	T1b	2
T3	u1	35	224PM3	5f	HV1	5	A3	T1c	3
T4	u1	36	224PM4	5h	HV1	5	A4	T1d	4
T5	v1	37	224PM5	6d	HV2	6	A5	T2a	5
T6	v1	38	224PM6	6e	HV2	6	A6	T2b	6
T7	v1	39	224PM7	6f	HV2	6	A7	T2c	7
T8	v1	40	224PM8	6f	HV2	6	A8	T2d	8
T9	u2	41	224PM9	7d	HV3	7	B1	T3a	9
T10	u2	42	224PM10	7e	HV3	7	B2	T3b	10
T11	u2	43	224PM11	7f	HV3	7	B3	T3c	11
T12	u2	44	224PM12	7h	HV3	7	B4	T3d	12
T13	u2	45	224PM13	8d	HV4	8	B5	T4a	12
T14	u2	46	224PM14	8e	HV4	8	B6	T4b	14
T15	u2	47	224PM15	8f	HV4	8	B7	T4c	15
T16	u2	48	224PM16	8h	HV4	8	B8	T4d	16

10) Trigger Condition

Cosmic Run

L1 = T1 or T2 or T3 or T4
L2 = T5 or T6 or T7 or T8
L3 = T9 or T10 or T11 or T12
L4 = T12 or T14 or T15 or T16

Trigger Pattern Bit TP0:	L1 and L2 and (L3 or L4)
Trigger Pattern Bit TP1:	L1 and L3 and (L2 or L4)
Trigger Pattern Bit TP2:	L1 and L4 and (L2 or L3)
Trigger Pattern Bit TP3:	L2 and L3 and (L1 or L4)
Trigger Pattern Bit TP4:	L2 and L4 and (L1 or L3)
Trigger Pattern Bit TP5:	L3 and L4 and (L1 or L2)
Trigger Pattern Bit TP6:	not used
Trigger Pattern Bit TP7:	L1 or L2 or L3 or L4

11) VFPS Multipurpose Cable

Connector 1: Rate Monitor Pot 220
Room 101: Connection to Rate Monitor
34 pol. Flat Cable Connector female
34 pol. Flat Cable, Length: 1 m
34 pol. Flat Cable Connector female
Tunnel: Connection to Trigger Board of Pot 220
34 pol. Flat Cable Connector female
34 pol. Flat Cable, Length: 2 m
34 pol. Flat Cable Connector female

Connector 2: Rate Monitor Pot 224
Room 101: Connection to Rate Monitor
34 pol. Flat Cable Connector female
34 pol. Flat Cable, Length: 1 m
34 pol. Flat Cable Connector female
Tunnel: Connection to Trigger Board of Pot 224
34 pol. Flat Cable Connector female
34 pol. Flat Cable, Length: 1 m
34 pol. Flat Cable Connector female

Connector 3:
Room 101: 34 pol. Flat Cable Connector female
20 pol. Flat Cable, 1 m, 25 pol. D-Sub Connector female (Switch Box)
10 pol. Flat Cable, 0,1 m, 10 pol. Flat Cable Conn. male (VME Scaler)
2 pol. Flat Cable, 0,05 m, 2 pol Pin Connector (Phone)
Tunnel: 34 pol. Flat Cable Connector female
20 pol. Flat Cable, 1 m, 20 pol. Flat Cable Conn. female (Temp. Mon.)
10 pol. Flat Cable, 0,1 m, 10 pol. Flat Cable Conn. male (Beam Monitor)
2 pol. Flat Cable, 0,05 m, 2 pol Pin Connector (Phone)

Connector 4: LED Pulse Generation
Room 101: Connection to LED Pulse Control Module
34 pol. Flat Cable Connector female
32 pol. Flat Cable, Length: 1 m
2 * 16 pol. Flat Cable Connector female
Tunnel: Connection to LED Driver Modules
34 pol. Flat Cable Connector female
32 pol. Flat Cable, Length: 1 m
2 * 16 pol. Flat Cable Connector female

Connector 5: Watch Dog
Room 101: Connection to Watch Dog Module
34 pol. Flat Cable Connector female
16 pol. Flat Cable, Length: 0,5 m
16 pol. Flat Cable Connector female
Tunnel: Connection to Motor Control Unit
34 pol. Flat Cable Connector female
16 pol. Flat Cable, Length: 3 m
15 pol. D-Sub Connector female